LP2997 DDR-II Termination Regulator

Check for Samples: LP2997

FEATURES

- Source and Sink Current
- Low Output Voltage Offset
- No External Resistors Required
- Linear Topology
- Suspend to Ram (STR) Functionality
- Low External Component Count
- Thermal Shutdown
- Available in SOIC-8, SO PowerPAD-8 Packages

APPLICATIONS

- DDR-II Termination Voltage
- SSTL-18 Termination

DESCRIPTION

The LP2997 linear regulator is designed to meet the JEDEC SSTL-18 specifications for termination of DDR-II memory. The device contains a high-speed operational amplifier to provide excellent response to load transients. The output stage prevents shoot through while delivering 500mA continuous current and transient peaks up to 900mA in the application as required for DDR-II SDRAM termination. The LP2997 also incorporates a V_{SENSE} pin to provide superior load regulation and a V_{REF} output as a reference for the chipset and DIMMs.

An additional feature found on the LP2997 is an active low shutdown ($\overline{SD}$) pin that provides Suspend To RAM (STR) functionality. When $\overline{SD}$ is pulled low the V_{TT} output will tri-state providing a high impedance output, but, V_{REF} will remain active. A power savings advantage can be obtained in this mode through lower quiescent current.

Typical Application Circuit

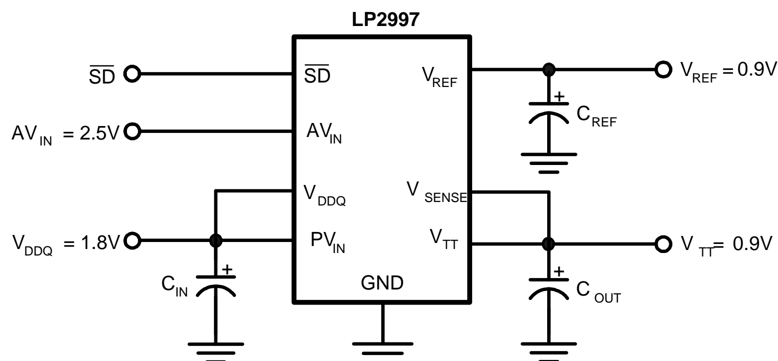

Figure 1. Typical Application Circuit

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Connection Diagram

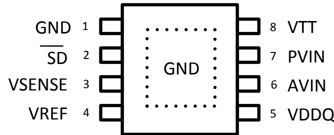

Figure 2. SO PowerPAD-8 Layout
See Package Number DDA (R-PDSO-G8)

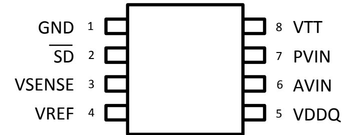

Figure 3. SOIC-8 Layout
See Package Number D0008A

PIN DESCRIPTIONS

SOIC-8 Pin or SO PowerPAD-8 Pin	Name	Function
1	GND	Ground
2	$\overline{SD}$	Shutdown
3	VSENSE	Feedback pin for regulating V_{TT}.
4	VREF	Buffered internal reference voltage of $V_{DDQ}/2$
5	VDDQ	Input for internal reference equal to $V_{DDQ}/2$
6	AVIN	Analog input pin
7	PVIN	Power input pin
8	VTT	Output voltage for connection to termination resistors
	EP	Exposed pad thermal connection Connect to Ground

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings(1)(2)

AVIN to GND	−0.3V to +6V
PVIN to GND	-0.3V to AVIN
VDDQ(3)	−0.3V to +6V
Storage Temp. Range	−65°C to +150°C
Junction Temperature	150°C
Lead Temperature (Soldering, 10 sec)	260°C
SOIC-8 Thermal Resistance ($θ_{JA}$)	151°C/W
SO PowerPAD-8 Thermal Resistance ($θ_{JA}$)	43°C/W
Minimum ESD Rating(4)	1kV

(1) Absolute maximum ratings indicate limits beyond which damage to the device may occur. Operating range indicates conditions for which the device is intended to be functional, but does not ensure specific performance limits. For specific specifications and test conditions see Electrical Characteristics. The specified specifications apply only for the test conditions listed. Some performance characteristics may degrade when the device is not operated under the listed test conditions.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) VDDQ voltage must be less than 2 x (AVIN - 1) or 6V, whichever is smaller.
(4) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin.

Operating Range

Junction Temp. Range(1)	0°C to +125°C
AVIN to GND	2.2V to 5.5V

(1) At elevated temperatures, devices must be derated based on thermal resistance. The device in the SOIC-8 package must be derated at $θ_{JA}$ = 151.2° C/W junction to ambient with no heat sink.

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Electrical Characteristics

Specifications with standard typeface are for T_J = 25°C and limits in **boldface type** apply over the full **Operating Temperature Range** (T_J = 0°C to +125°C)(1). Unless otherwise specified, AVIN = 2.5V, PVIN = 1.8V, VDDQ = 1.8V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
V_{REF}	V_{REF} Voltage	PVIN = VDDQ = 1.7V PVIN = VDDQ = 1.8V PVIN = VDDQ = 1.9V	**0.837** **0.887** **0.936**	0.860 0.910 0.959	**0.887** **0.937** **0.986**	V
Z_{VREF}	V_{REF} Output Impedance	I_{REF} = -30 to +30 µA		2.5		kΩ
V_{TT}	V_{TT} Output Voltage	I_{OUT} = 0A PVIN = VDDQ = 1.7V PVIN = VDDQ = 1.8V PVIN = VDDQ = 1.9V	 **0.822** **0.874** **0.923**	 0.856 0.908 0.957	 **0.887** **0.939** **0.988**	V
		I_{OUT} = ±0.5A(2) PVIN = VDDQ = 1.7V PVIN = VDDQ = 1.8V PVIN = VDDQ = 1.9V	 **0.828** **0.878** **0.928**	 0.856 0.908 0.957	 **0.890** **0.940** **0.990**	
Vos_{TT}/V_{TT}	V_{TT} Output Voltage Offset (V_{REF}-V_{TT})	I_{OUT} = 0A I_{OUT} = -0.5A I_{OUT} = +0.5A	**-25** **-25** **-25**	0 0 0	**25** **25** **25**	mV
I_Q	Quiescent Current(3)	I_{OUT} = 0A(3)		320	**500**	µA
Z_{VDDQ}	VDDQ Input Impedance			100		kΩ
I_{SD}	Quiescent Current in Shutdown(3)	SD = 0V		115	**150**	µA
I_{Q_SD}	Shutdown Leakage Current	SD = 0V		2	**5**	µA
V_{IH}	Minimum Shutdown High Level		**1.9**			V
V_{IL}	Maximum Shutdown Low Level				**0.8**	V
I_{SENSE}	V_{SENSE} Input Current			13		nA
T_{SD}	Thermal Shutdown	See(4)		165		Celsius
$T_{SD_}$HYS	Thermal Shutdown Hysteresis			10		Celsius

(1) Limits are 100% production tested at 25°C. Limits over the operating temperature range are specified through correlation using Statistical Quality Control (SQC) methods. The limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) V_{TT} load regulation is tested by using a 10 ms current pulse and measuring V_{TT}.
(3) Quiescent current defined as the current flow into AVIN.
(4) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction to ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. Exceeding the maximum allowable power dissipation will cause excessive die temperature and the regulator will go into thermal shutdown.

Typical Performance Characteristics

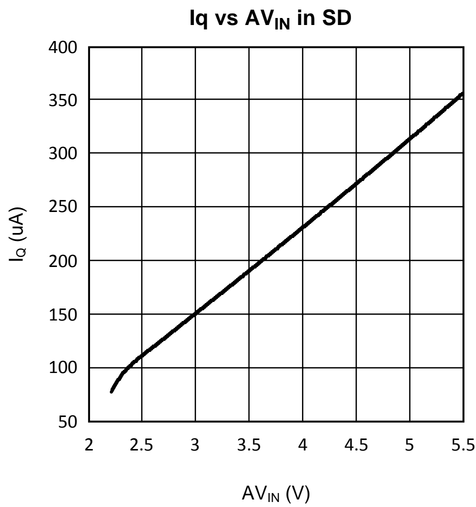

Figure 4.

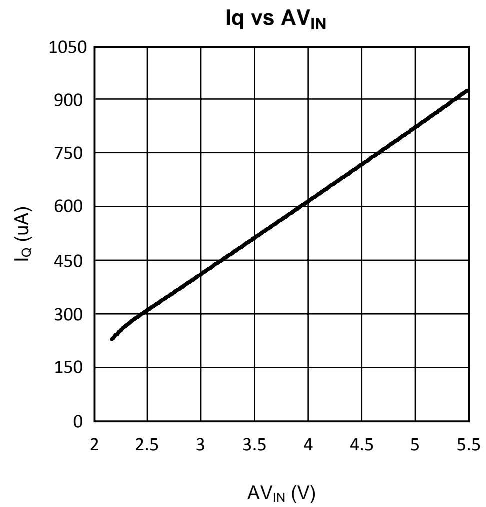

Figure 5.

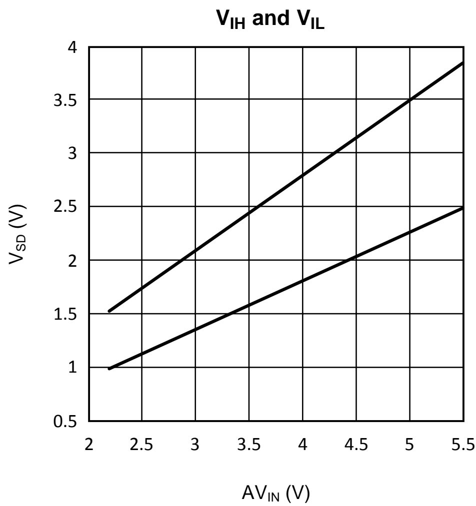

Figure 6.

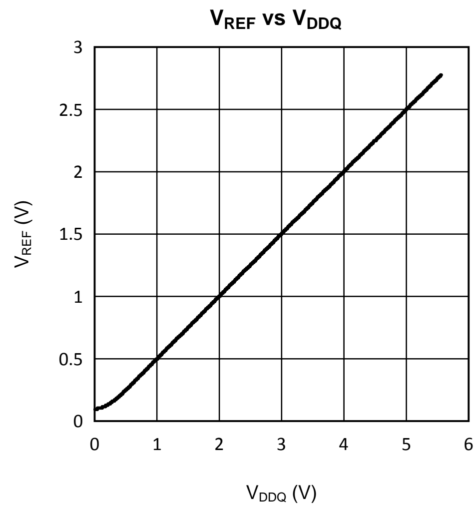

Figure 7.

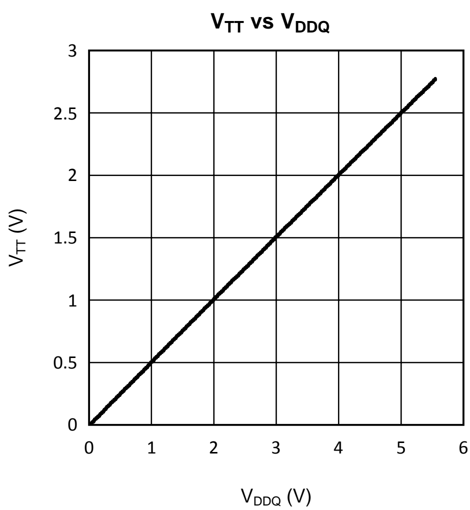

Figure 8.

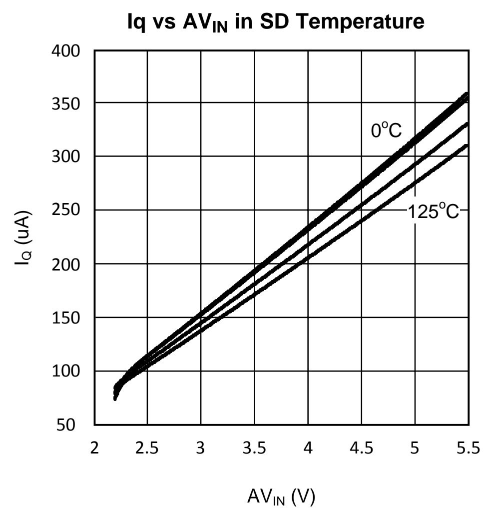

Figure 9.

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Typical Performance Characteristics (continued)

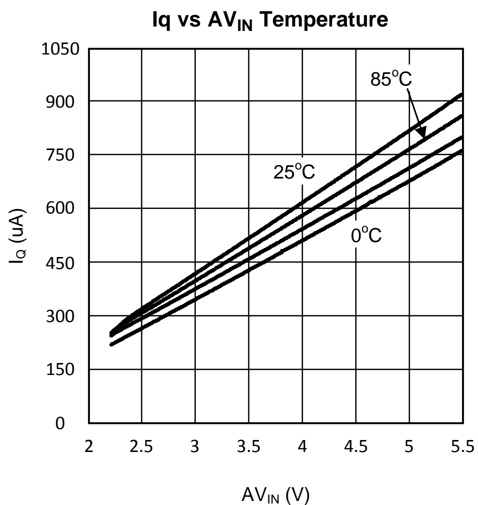


Figure 10.

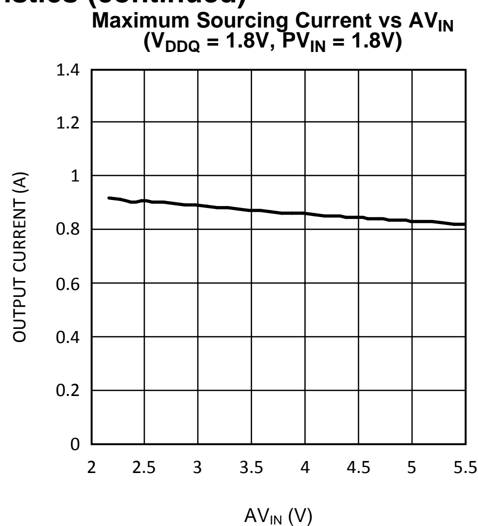


Figure 11.

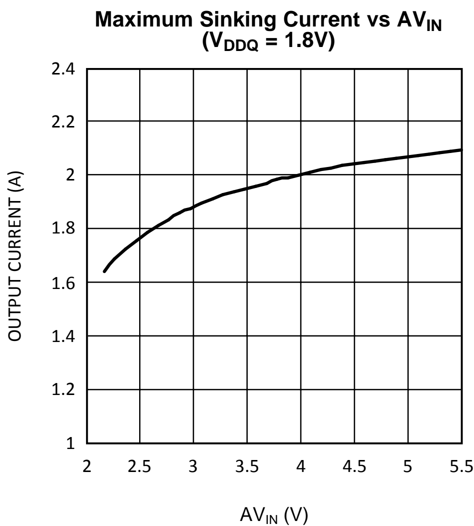
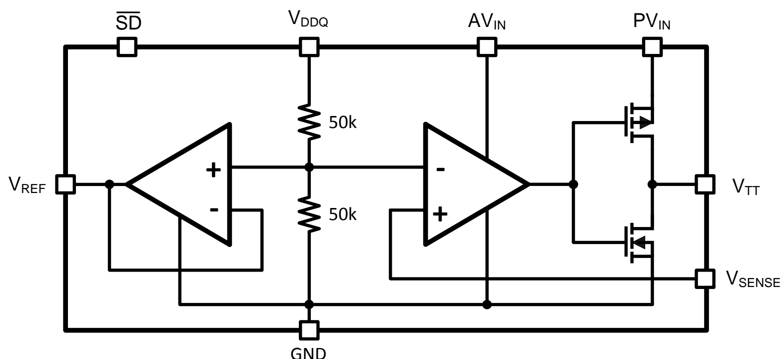


Figure 12.

Block Diagram



DESCRIPTION

The LP2997 is a linear bus termination regulator designed to meet the JEDEC requirements of SSTL-18. The output, V_{TT} is capable of sinking and sourcing current while regulating the output voltage equal to VDDQ / 2. The output stage has been designed to maintain excellent load regulation while preventing shoot through. The LP2997 also incorporates two distinct power rails that separates the analog circuitry from the power output stage. This allows a split rail approach to be utilized to decrease internal power dissipation. It also permits the LP2997 to provide a termination solution for the next generation of DDR-SDRAM memory (DDRII).

Pin Descriptions

AVIN AND PVIN AVIN and PVIN are the input supply pins for the LP2997. AVIN is used to supply all the internal control circuitry. PVIN, however, is used exclusively to provide the rail voltage for the output stage used to create V_{TT}. These pins have the capability to work off separate supplies, under the condition that AVIN is always greater than or equal to PVIN. For SSTL-18 applications, it is recommended to connect PVIN to the 1.8V rail used for the memory core and AVIN to a rail within its operating range of 2.2V to 5.5V (typically a 2.5V supply). PVIN should always be used with either a 1.8V or 2.5V rail. This prevents the thermal limit from tripping because of excessive internal power dissipation. If the junction temperature exceeds the thermal shutdown than the part will enter a shutdown state identical to the manual shutdown where V_{TT} is tri-stated and V_{REF} remains active. A lower rail such as 1.5V can be used but it will reduce the maximum output current, therefore it is not recommended for most termination schemes.

VDDQ VDDQ is the input used to create the internal reference voltage for regulating V_{TT}. The reference voltage is generated from a resistor divider of two internal 50kΩ resistors. This ensures that V_{TT} will track VDDQ / 2 precisely. The optimal implementation of VDDQ is as a remote sense. This can be achieved by connecting VDDQ directly to the 1.8V rail at the DIMM instead of PVIN. This ensures that the reference voltage tracks the DDR memory rails precisely without a large voltage drop from the power lines. For SSTL-18 applications VDDQ will be a 1.8V signal, which will create a 0.9V termination voltage at V_{TT} (See Electrical Characteristics Table for exact values of V_{TT} over temperature).

V_{SENSE} The purpose of the sense pin is to provide improved remote load regulation. In most motherboard applications the termination resistors will connect to V_{TT} in a long plane. If the output voltage was regulated only at the output of the LP2997 then the long trace will cause a significant IR drop resulting in a termination voltage lower at one end of the bus than the other. The V_{SENSE} pin can be used to improve this performance, by connecting it to the middle of the bus. This will provide a better distribution across the entire termination bus. If remote load regulation is not used then the V_{SENSE} pin must still be connected to V_{TT}. Care should be taken when a long V_{SENSE} trace is implemented in close proximity to the memory. Noise pickup in the V_{SENSE} trace can cause problems with precise regulation of V_{TT}. A small 0.1uF ceramic capacitor placed next to the V_{SENSE} pin can help filter any high frequency signals and preventing errors.

SHUTDOWN The LP2997 contains an active low shutdown pin that can be used for suspend to RAM functionality. In this condition the V_{TT} output will tri-state while the V_{REF} output remains active providing a constant reference signal for the memory and chipset. During shutdown V_{TT} should not be exposed to voltages that exceed PVIN. With the shutdown pin asserted low the quiescent current of the LP2997 will drop, however, VDDQ will always maintain its constant impedance of 100kΩ for generating the internal reference. Therefore, to calculate the total power loss in shutdown both currents need to be considered. For more information refer to the Thermal Dissipation section. The shutdown pin also has an internal pull-up current; therefore, to turn the part on the shutdown pin can either be connected to AVIN or left open

V_{REF} V_{REF} provides the buffered output of the internal reference voltage VDDQ / 2. This output should be used to provide the reference voltage for the Northbridge chipset and memory. Since these inputs are typically an extremely high impedance, there should be little current drawn from V_{REF}. For improved performance, an output bypass capacitor can be used, located close to the pin, to help with noise. A ceramic capacitor in the range of 0.1 µF to 0.01 µF is recommended. This output remains active during the shutdown state and thermal shutdown events for the suspend to RAM functionality.

V_{TT} V_{TT} is the regulated output that is used to terminate the bus resistors. It is capable of sinking and sourcing current while regulating the output precisely to VDDQ / 2. The LP2997 is designed to handle continuous currents of up to +/- 0.5A with excellent load regulation. If a transient is expected to last above the maximum continuous current rating for a significant amount of time, then the bulk output capacitor should be sized large enough to prevent an excessive voltage drop. If the LP2997 is to operate in elevated temperatures for long durations care should be taken to ensure that the maximum junction temperature is not exceeded. Proper thermal de-rating should always be used. (Please refer to the Thermal Dissipation section) If the junction temperature exceeds the thermal shutdown point than V_{TT} will tri-state until the part returns below the temperature hysteresis trip-point

COMPONENT SELECTIONS

INPUT CAPACITOR

The LP2997 does not require a capacitor for input stability, but it is recommended for improved performance during large load transients to prevent the input rail from dropping. The input capacitor should be located as close as possible to the PVIN pin. Several recommendations exist dependent on the application required. A typical value recommended for AL electrolytic capacitors is 22 µF. Ceramic capacitors can also be used. A value in the range of 10 µF with X5R or better would be an ideal choice. The input capacitance can be reduced if the LP2997 is placed close to the bulk capacitance from the output of the 1.8V DC-DC converter. For the AVIN pin, a small 0.1uF ceramic capacitor is sufficient to prevent excessive noise from coupling into the device.

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OUTPUT CAPACITOR

The LP2997 has been designed to be insensitive of output capacitor size or ESR (Equivalent Series Resistance). This allows the flexibility to use any capacitor desired. The choice for output capacitor will be determined solely on the application and the requirements for load transient response of V_{TT}. As a general recommendation the output capacitor should be sized above 100 µF with a low ESR for SSTL applications with DDR-SDRAM. The value of ESR should be determined by the maximum current spikes expected and the extent at which the output voltage is allowed to droop. Several capacitor options are available on the market and a few of these are highlighted below:

AL - It should be noted that many aluminum electrolytics only specify impedance at a frequency of 120 Hz, which indicates they have poor high frequency performance. Only aluminum electrolytics that have an impedance specified at a higher frequency (100 kHz) should be used for the LP2997. To improve the ESR several AL electrolytics can be combined in parallel for an overall reduction. An important note to be aware of is the extent at which the ESR will change over temperature. Aluminum electrolytic capacitors can have their ESR rapidly increase at cold temperatures.

Ceramic - Ceramic capacitors typically have a low capacitance, in the range of 10 to 100 µF range, but they have excellent AC performance for bypassing noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature. Because of the typically low value of capacitance it is recommended to use ceramic capacitors in parallel with another capacitor such as an aluminum electrolytic. A dielectric of X5R or better is recommended for all ceramic capacitors.

Hybrid - Several hybrid capacitors such as OS-CON and SP are available from several manufacturers. These offer a large capacitance while maintaining a low ESR. These are the best solution when size and performance are critical, although their cost is typically higher than any other capacitors.

Thermal Dissipation

Since the LP2997 is a linear regulator any current flow from V_{TT} will result in internal power dissipation generating heat. To prevent damaging the part from exceeding the maximum allowable junction temperature, care should be taken to derate the part dependent on the maximum expected ambient temperature and power dissipation. The maximum allowable internal temperature rise (T_{Rmax}) can be calculated given the maximum ambient temperature (T_{Amax}) of the application and the maximum allowable junction temperature (T_{Jmax}).

$$T_{Rmax} = T_{Jmax} - T_{Amax} \quad (1)$$

From this equation, the maximum power dissipation (P_{Dmax}) of the part can be calculated:

$$P_{Dmax} = T_{Rmax} / \theta_{JA} \quad (2)$$

The θ_{JA} of the LP2997 will be dependent on several variables: the package used; the thickness of copper; the number of vias and the airflow. For instance, the θ_{JA} of the SOIC-8 is 163°C/W with the package mounted to a standard 8x4 2-layer board with 1oz. copper, no airflow, and 0.5W dissipation at room temperature. This value can be reduced to 151.2°C/W by changing to a 3x4 board with 2 oz. copper that is the JEDEC standard. Figure 13 shows how the θ_{JA} varies with airflow for the two boards mentioned.

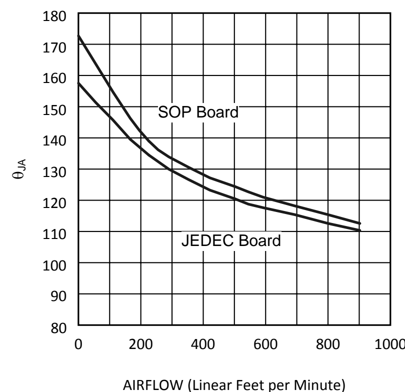

Figure 13. θ_{JA} vs Airflow (SOIC-8)

Additional improvements can be made by the judicious use of vias to connect the part and dissipate heat to an internal ground plane. Using larger traces and more copper on the top side of the board can also help. With careful layout it is possible to reduce the θ_{JA} further than the nominal values shown in Figure 13.

Optimizing the θ_{JA} and placing the LP2997 in a section of a board exposed to lower ambient temperature allows the part to operate with higher power dissipation. The internal power dissipation can be calculated by summing the three main sources of loss: output current at V_{TT}, either sinking or sourcing, and quiescent current at AVIN and VDDQ. During the active state (when shutdown is not held low) the total internal power dissipation can be calculated from the following equations:

$$P_D = P_{AVIN} + P_{VDDQ} + P_{VTT} \quad (3)$$

Where,

$$P_{AVIN} = I_{AVIN} * V_{AVIN} \quad (4)$$

$$P_{VDDQ} = V_{VDDQ} * I_{VDDQ} = V_{VDDQ}^2 \text{ x } R_{VDDQ} \quad (5)$$

To calculate the maximum power dissipation at V_{TT} both conditions at V_{TT} need to be examined, sinking and sourcing current. Although only one equation will add into the total, V_{TT} cannot source and sink current simultaneously.

$$P_{VTT} = V_{VTT} \text{ x } I_{LOAD} \text{ (Sinking) or} \quad (6)$$

$$P_{VTT} = (V_{PVIN} - V_{VTT}) \text{ x } I_{LOAD} \text{ (Sourcing)} \quad (7)$$

The power dissipation of the LP2997 can also be calculated during the shutdown state. During this condition the output V_{TT} will tri-state, therefore that term in the power equation will disappear as it cannot sink or source any current (leakage is negligible). The only losses during shutdown will be the reduced quiescent current at AVIN and the constant impedance that is seen at the VDDQ pin.

$$P_D = P_{AVIN} + P_{VDDQ} \quad (8)$$

$$P_{AVIN} = I_{AVIN} \text{ x } V_{AVIN} \quad (9)$$

$$P_{VDDQ} = V_{VDDQ} * I_{VDDQ} = V_{VDDQ}^2 \text{ x } R_{VDDQ} \quad (10)$$

Typical Application Circuits

Several different application circuits have been shown to illustrate some of the options that are possible in configuring the LP2997. Graphs of the individual circuit performance can be found in the Typical Performance Characteristics section in the beginning of the datasheet. These curves illustrate how the maximum output current is affected by changes in AVIN and PVIN.

Figure 14 shows the recommended circuit configuration for DDR-II applications. The output stage is connected to the 1.8V rail and the AVIN pin can be connected to either a 2.5V, 3.3V or 5V rail.

This circuit permits termination in a minimum amount of board space and component count. Capacitor selection can be varied depending on the number of lines terminated and the maximum load transient. However, with motherboards and other applications where V_{TT} is distributed across a long plane it is advisable to use multiple bulk capacitors and addition to high frequency decoupling. The bulk output capacitors should be situated at both ends of the V_{TT} plane for optimal placement. Large aluminum electrolytic capacitors are used for their low ESR and low cost.

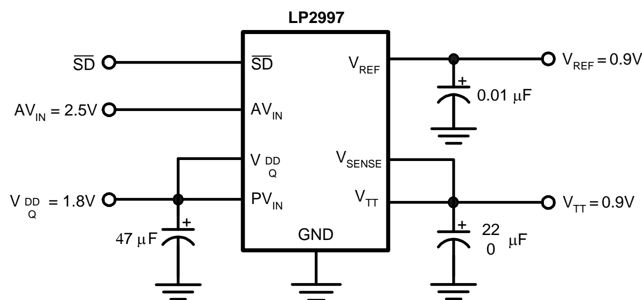

Figure 14. Recommended DDR-II Termination

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PCB Layout Considerations

1. The input capacitor for the power rail should be placed as close as possible to the PVIN pin.
2. V_{SENSE} should be connected to the V_{TT} termination bus at the point where regulation is required. For motherboard applications an ideal location would be at the center of the termination bus.
3. V_{DDQ} can be connected remotely to the V_{DDQ} rail input at either the DIMM or the Chipset. This provides the most accurate point for creating the reference voltage.
4. For improved thermal performance excessive top side copper should be used to dissipate heat from the package. Numerous vias from the ground connection to the internal ground plane will help. Additionally these can be located underneath the package if manufacturing standards permit.
5. Care should be taken when routing the V_{SENSE} trace to avoid noise pickup from switching I/O signals. A 0.1uF ceramic capacitor located close to the $_{SENSE}$ can also be used to filter any unwanted high frequency signal. This can be an issue especially if long $_{SENSE}$ traces are used.
6. V_{REF} should be bypassed with a 0.01 μF or 0.1 μF ceramic capacitor for improved performance. This capacitor should be located as close as possible to the V_{REF} pin.

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REVISION HISTORY

Changes from Revision E (April 2013) to Revision F	Page
• Changed layout of National Data Sheet to TI format	9

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP2997M	NRND	SOIC	D	8	95	TBD	Call TI	Call TI	0 to 125	L2997 M	
LP2997M/NOPB	ACTIVE	SOIC	D	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 125	L2997 M	Samples
LP2997MR	NRND	SO PowerPAD	DDA	8	95	TBD	Call TI	Call TI	0 to 125	L2997 MR	
LP2997MR/NOPB	ACTIVE	SO PowerPAD	DDA	8	95	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	L2997 MR	Samples
LP2997MRX	NRND	SO PowerPAD	DDA	8	2500	TBD	Call TI	Call TI	0 to 125	L2997 MR	
LP2997MRX/NOPB	ACTIVE	SO PowerPAD	DDA	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-3-260C-168 HR	0 to 125	L2997 MR	Samples
LP2997MX/NOPB	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	0 to 125	L2997 M	Samples

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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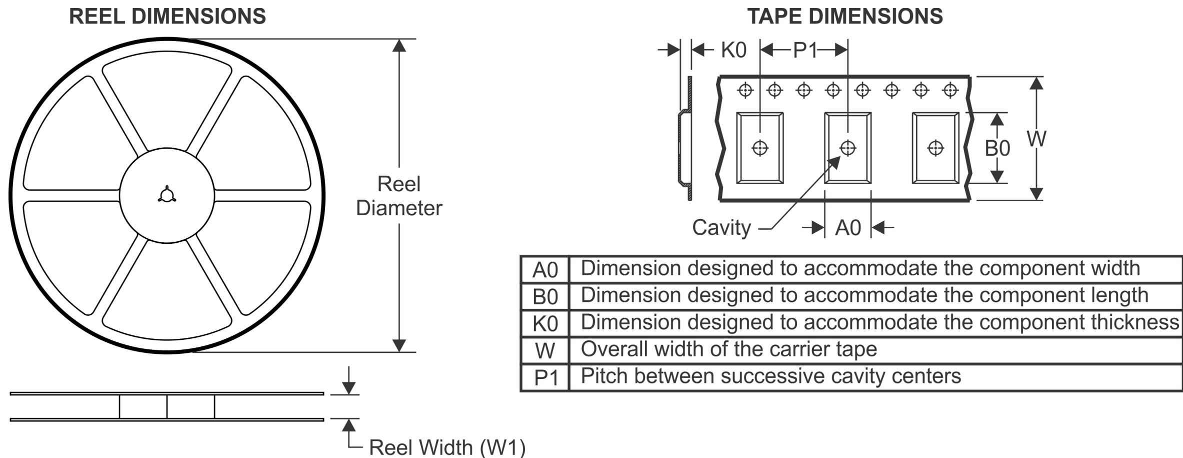
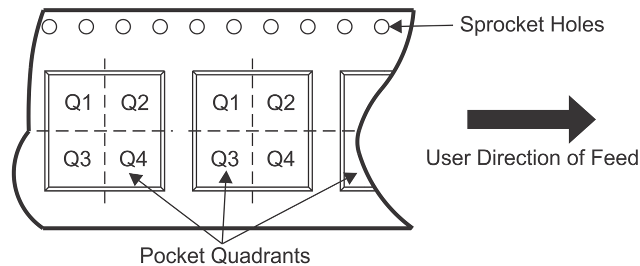
TAPE AND REEL INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

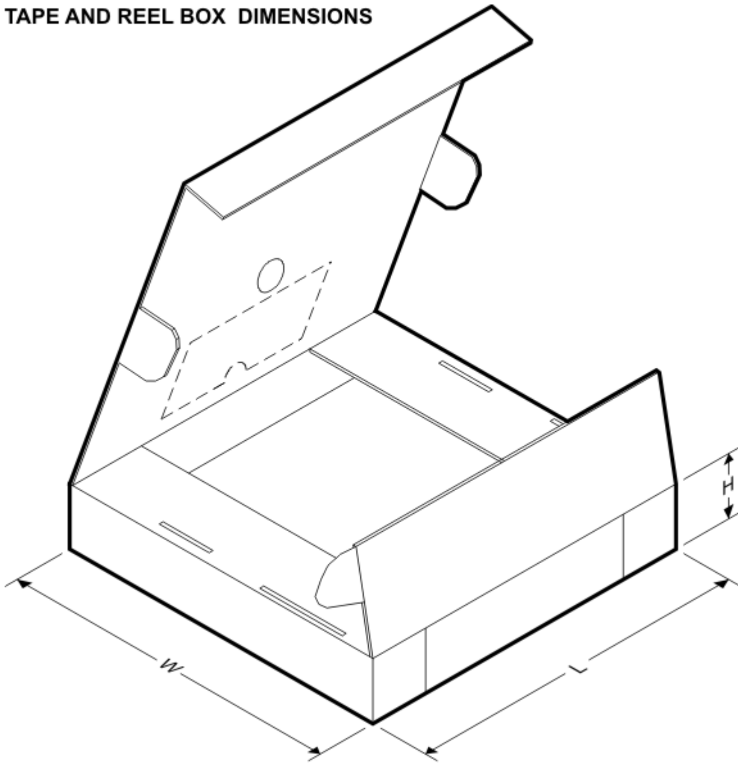
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP2997MRX	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2997MRX/NOPB	SO Power PAD	DDA	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1
LP2997MX/NOPB	SOIC	D	8	2500	330.0	12.4	6.5	5.4	2.0	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP2997MRX	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LP2997MRX/NOPB	SO PowerPAD	DDA	8	2500	367.0	367.0	35.0
LP2997MX/NOPB	SOIC	D	8	2500	367.0	367.0	35.0

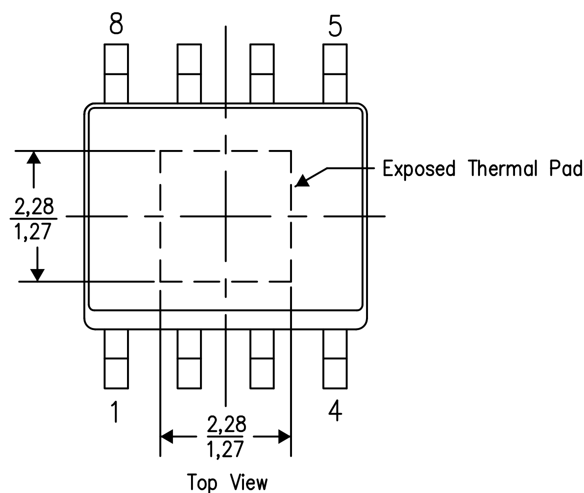
DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



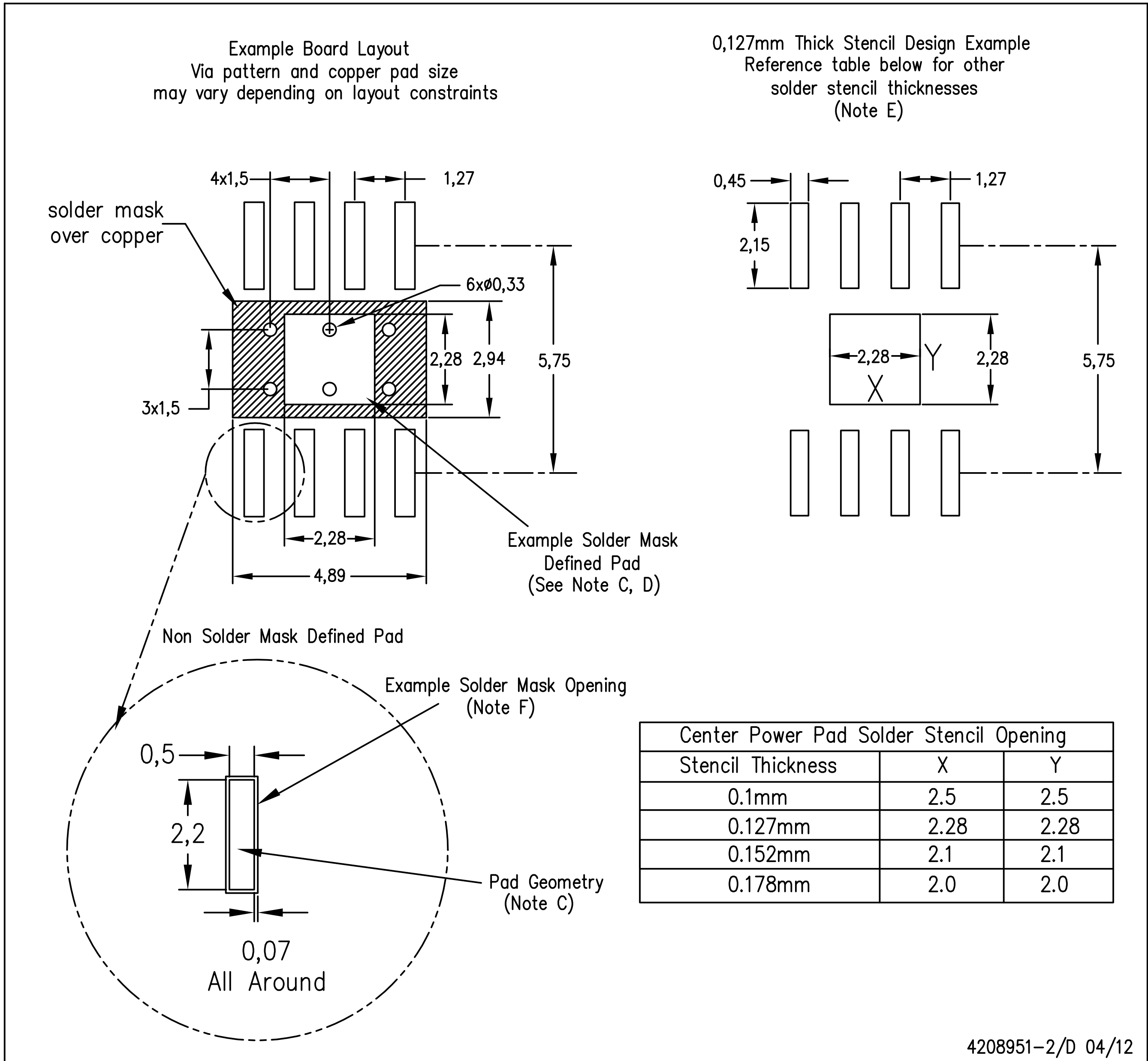
Exposed Thermal Pad Dimensions

4206322-2/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DDA (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.5
0.127mm	2.28	2.28
0.152mm	2.1	2.1
0.178mm	2.0	2.0

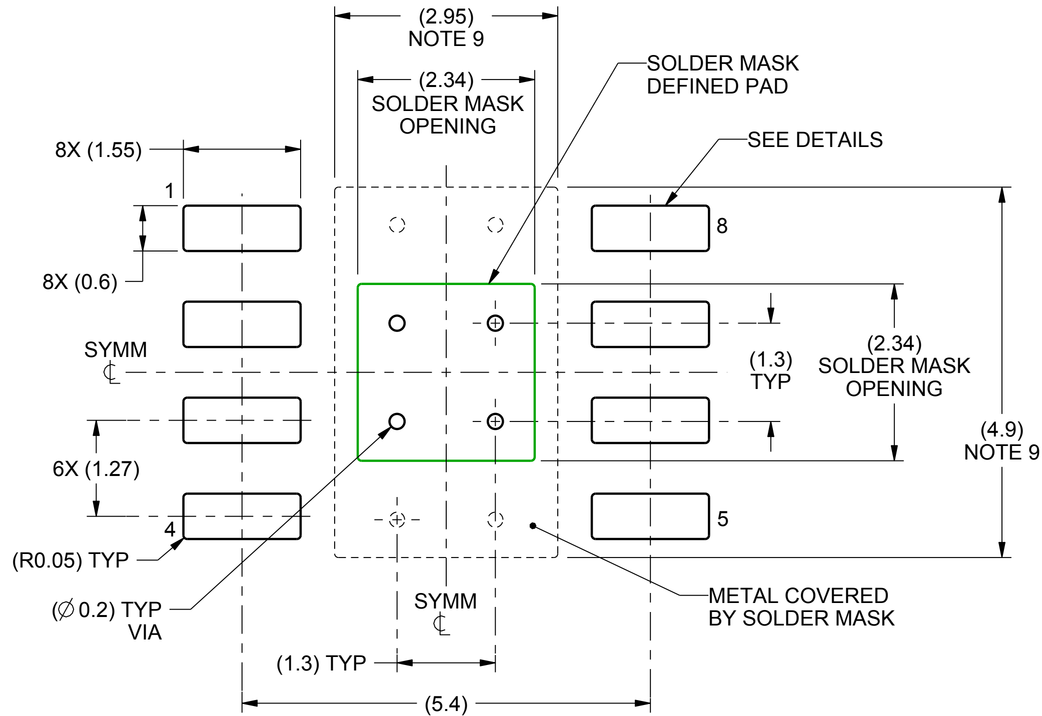
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC-7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC-7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

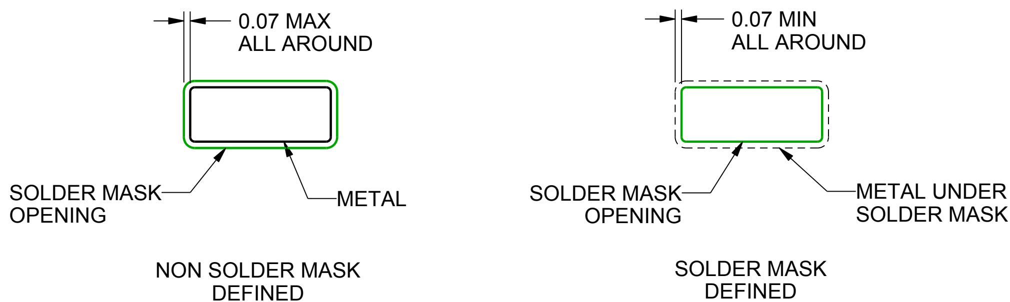
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MS-012.



LAND PATTERN EXAMPLE
SCALE:10X



NON SOLDER MASK DEFINED

SOLDER MASK DEFINED

SOLDER MASK DETAILS

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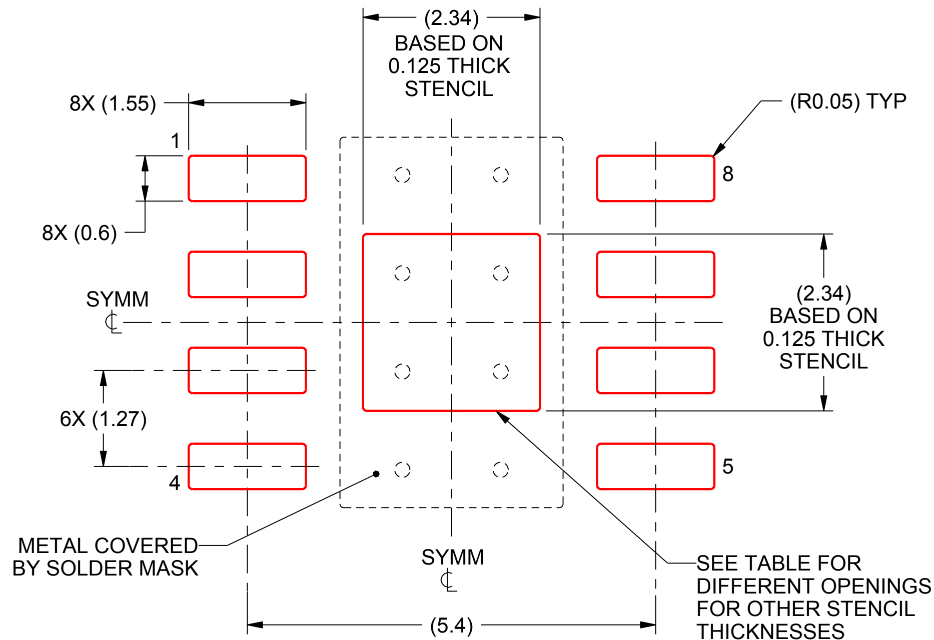
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
EXPOSED PAD
100% PRINTED SOLDER COVERAGE BY AREA
SCALE:10X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	2.62 X 2.62
0.125	2.34 X 2.34 (SHOWN)
0.150	2.14 X 2.14
0.175	1.98 X 1.98

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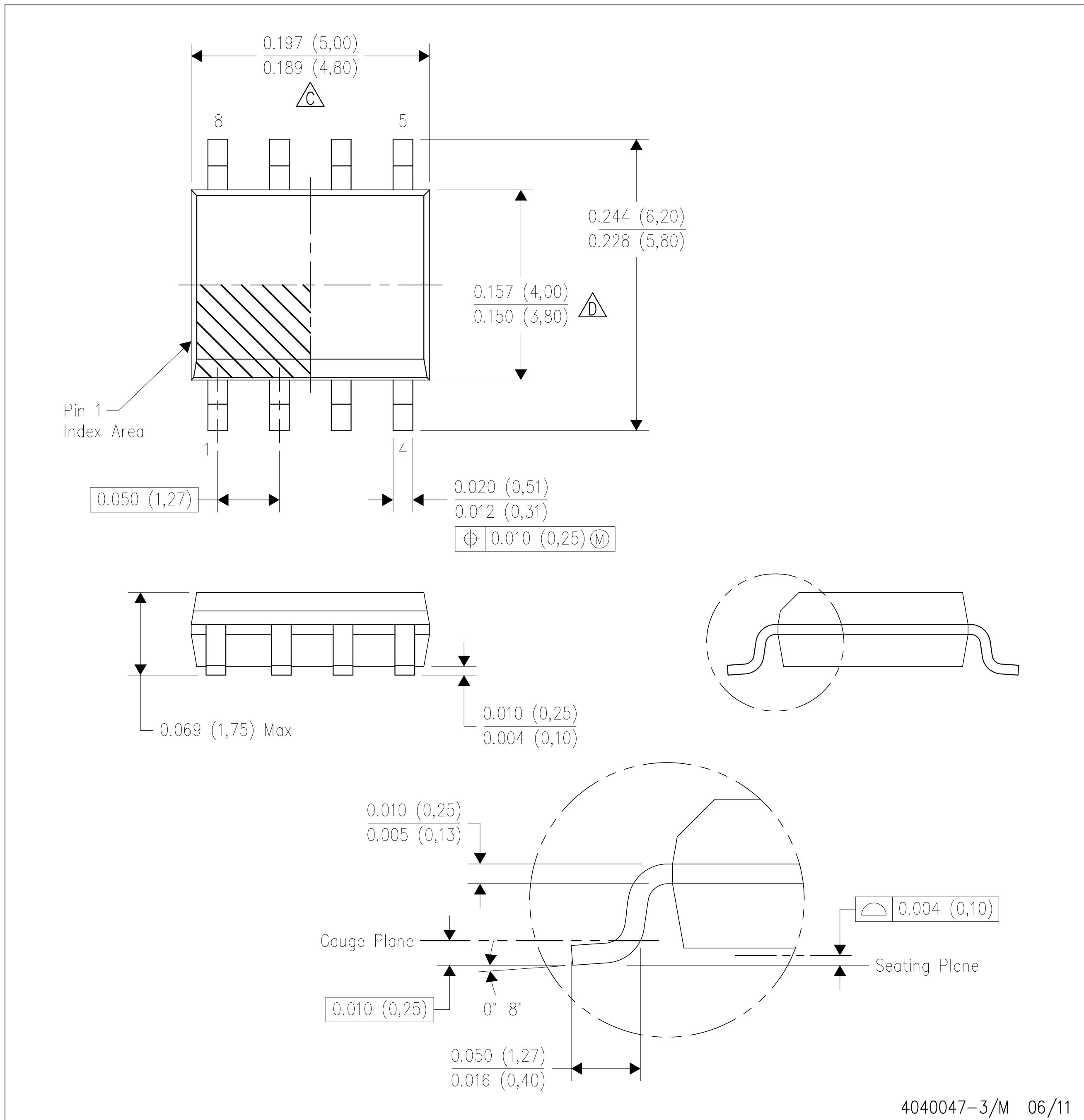
NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

D (R–PDSO–G8) PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AA.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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