

Sample &

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TLC555

Reference

Design

TLC555 LinCMOS[™] Timer

Technical

Documents

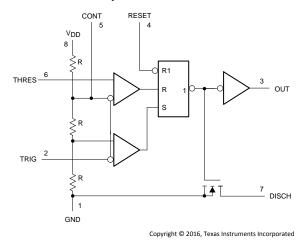
1 Features

- Very Low Power Consumption:
 - 1 mW Typical at V_{DD} = 5 V
- Capable of Operation in Astable Mode
- CMOS Output Capable of Swinging Rail to Rail
- High Output Current Capability
 - Sink: 100 mA Typical
 - Source: 10 mA Typical
- Output Fully Compatible With CMOS, TTL, and MOS
- Low Supply Current Reduces Spikes During **Output Transitions**
- Single-Supply Operation From 2 V to 15 V
- Functionally Interchangeable With the NE555; Has Same Pinout
- ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015.2
- Available in Q-Temp Automotive
 - High-Reliability Automotive Applications
 - Configuration Control and Print Support
 - Qualification to Automotive Standards

2 Applications

- **Precision Timing**
- Pulse Generation
- Sequential Timing
- **Time Delay Generation**
- Pulse Width Modulation
- **Pulse Position Modulation**
- Linear Ramp Generator

Simplified Schematic



3 Description

Tools &

Software

The TLC555 is a monolithic timing circuit fabricated using the TI LinCMOS[™] process. The timer is fully compatible with CMOS, TTL, and MOS logic, and operates at frequencies up to 2 MHz. Because of its high input impedance, this device uses smaller timing capacitors than those used by the NE555. As a result, more accurate time delays and oscillations are possible. Power consumption is low across the full range of power-supply voltage.

Support &

Community

SLFS043H-SEPTEMBER 1983-REVISED AUGUST 2016

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Like the NE555, the TLC555 has a trigger level equal to approximately one-third of the supply voltage and a threshold level equal to approximately two-thirds of the supply voltage. These levels can be altered by use of the control voltage terminal (CONT). When the trigger input (TRIG) falls below the trigger level, the flip-flop is set and the output goes high. If TRIG is above the trigger level and the threshold input (THRES) is above the threshold level, the flip-flop is reset and the output is low. The reset input (RESET) can override all other inputs and can be used to initiate a new timing cycle. If RESET is low, the flipflop is reset and the output is low. Whenever the output is low, a low-impedance path is provided between the discharge terminal (DISCH) and GND. All unused inputs must be tied to an appropriate logic level to prevent false triggering.

Device information '							
PACKAGE	BODY SIZE (NOM)						
SOIC (8)	4.9 mm × 3.91 mm						
PDIP (8)	9.81 mm × 6.38 mm						
SOP (8)	6.20 mm × 5.30 mm						
TSSOP (14)	5.00 mm × 4.40 mm						
SOIC (8)	4.90 mm × 3.91 mm						
PDIP (8)	9.81 mm × 6.38 mm						
LCCC (20)	8.89 mm × 8.89 mm						
CDIP (8)	9.60 mm × 6.67 mm						
SOIC (8)	4.90 mm × 3.91 mm						
	PACKAGE SOIC (8) PDIP (8) SOP (8) TSSOP (14) SOIC (8) PDIP (8) LCCC (20) CDIP (8)						

Device Information⁽¹⁾

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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Mechanical, Packaging, and Orderable

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4 Revision History

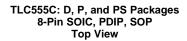
Cł	nanges from Revision G (November 2008) to Revision H	Page
•	Added Feature Description section, Device Functional Modes, Application and Implementation section, Power Supply Recommendations section, Layout section, Device and Documentation Support section, and Mechanical, Packaging, and Orderable Information section	1
•	Deleted Continuous total power dissipation and lead temperature parameters from Absolute Maximum Ratings	6
•	Changed values in the Thermal Information table to align with JEDEC standards	6
•	Deleted Dissipation Ratings table	6

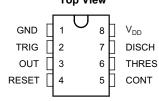
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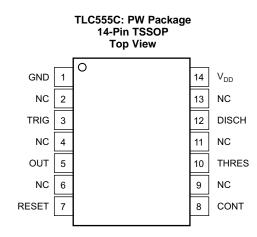
5 Device Comparison Table

DEVICE	T _A	V _{DD} RANGE	SMALL OUTLINE (D)	CHIP CARRIER (FK)	CERAMIC DIP (JG)	PLASTIC DIP (P)	SSOP (PS)	TSSOP (PW)
TLC555C	0°C to 70°C	2 V to 15 V	✓	—	—	1	1	\checkmark
TLC555I	–40°C to 85°C	3 V to 15 V	\checkmark	—	—	1	—	—
TLC555M	–55°C to 125°C	5 V to 15 V	_	1	1	_	_	_
TLC555Q	–40°C to 125°C	5 V to 15 V	~	—	—	—	—	—

6 Pin Configuration and Functions







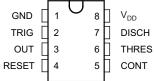
Pin Functions: TLC555C

	PIN			
NAME	SOIC, PDIP, SOP	TSSOP	I/O	DESCRIPTION
CONT	5	8	I	Controls comparator thresholds. Outputs 2/3 V_{DD} and allows bypass capacitor connection.
DISCH	7	12	0	Open collector output to discharge timing capacitor
GND	1	1		Ground
NC	_	2, 4, 6, 9, 11, 13	—	No internal connection
OUT	3	5	0	High current timer output signal
RESET	4	7	I	Active low reset input forces output and discharge low
THRES	6	10	I	End of timing input. THRES > CONT sets output low and discharge low.
TRIG	2	3	I	Start of timing input. TRIG < 1/2 CONT sets output high and discharge open.
V _{DD}	8	14	_	Power-supply voltage

TEXAS INSTRUMENTS

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TLC555I: D and P Packages 8-Pin SOIC, PDIP Top View

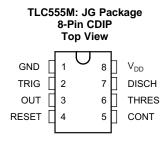


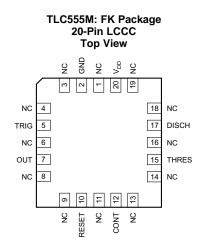
Pin Functions: TLC555I

Р	IN	I/O	DESCRIPTION
NAME	SOIC, PDIP	1/0	DESCRIPTION
CONT	5	I	Controls comparator thresholds. Outputs 2/3 V_{DD} and allows bypass capacitor connection.
DISCH	7	0	Open-collector output to discharge timing capacitor
GND	1	_	Ground
OUT	3	0	High current timer output signal
RESET	4	Ι	Active low reset input forces output and discharge low
THRES	6	Ι	End of timing input. THRES > CONT sets output low and discharge low.
TRIG	2	Ι	Start of timing input. TRIG < 1/2 CONT sets output high and discharge open.
V _{DD}	8	_	Power-supply voltage

4



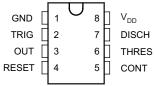




Pin Functions: TLC555M

	PIN		1/0	DESCRIPTION
NAME	LCCC	CDIP	1/0	DESCRIPTION
CONT	12	5	I	Controls comparator thresholds. Outputs 2/3 V_{DD} and allows bypass capacitor connection.
DISCH	17	7	0	Open-collector output to discharge timing capacitor
GND	2	1	—	Ground
NC	1, 3, 4, 6, 8, 9, 11, 13, 14, 16, 18, 19	_	_	No internal connection
OUT	7	3	0	High current timer output signal
RESET	10	4	I	Active low reset input forces output and discharge low
THRES	15	6	I	End of timing input. THRES > CONT sets output low and discharge low.
TRIG	5	2	I	Start of timing input. TRIG < 1/2 CONT sets output high and discharge open.
V _{DD}	20	8	—	Power-supply voltage

TLC555Q: D Package 8-Pin SOIC Top View



Pin Functions: TLC555Q

	PIN	- <i>V</i> O	DESCRIPTION
NAME	SOIC	1/0	DESCRIPTION
CONT	5	I	Controls comparator thresholds, Outputs 2/3 VDD, allows bypass capacitor connection
DISCH	7	0	Open-collector output to discharge timing capacitor
GND	1	_	Ground
OUT	3	0	High current timer output signal
RESET	4	I	Active low reset input forces output and discharge low
THRES	6	I	End of timing input. THRES > CONT sets output low and discharge low
TRIG	2	I	Start of timing input. TRIG < 1/2 CONT sets output high and discharge open
V _{DD}	8	_	Power supply voltage

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
Voltage Current Temperature	Supply, V _{DD} ⁽²⁾		18	V	
	Input, any input	-0.3	V _{DD}	V	
Current	Sink, discharge or output		150	mA	
	Source, output, I _O		15	mA	
	Operating, T _A	C-suffix	0	70	°C
		I-suffix	-40	85	°C
Tomporatura		Q-suffix	-40	125	°C
Temperature		M-suffix	-55	125	°C
	Case, for 60 seconds	FK package	-65	150	°C
	Storage, T _{stg}		-65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) All voltage values are with respect to network GND.

7.2 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Supply voltage, V _{DD} TLC555C Operating free-air temperature, T _A TLC555M		2	15	V
TLOS	TLC555C	0	70	°C
	TLC555I	-40	85	°C
temperature, T _A	TLC555M	-55	15 V 70 °C	
	TLC555Q	-40	125	°C

7.3 Thermal Information

		TLC555						
THERMAL METRIC ⁽¹⁾		D (SOIC)	FK (LCCC)	JG (CDIP)	P (PDIP)	PS (SOP)	PW (TSSOP)	UNIT
		8 PINS	20 PINS	8 PINS	8 PINS	8 PINS	14 PINS	Ī
$R_{\theta JA}$	Junction-to-ambient thermal resistance	113	n/a	120	58	120	135	°C/W
R _{0JC(top)}	Junction-to-case (top) thermal resistance	58	37	81	48	72	61	°C/W
R _{0JB}	Junction-to-board thermal resistance	55	36	110	35	69	77	°C/W
ΨJT	Junction-to-top characterization parameter	11	n/a	45	26	32	12	°C/W
ΨJB	Junction-to-board characterization parameter	54	n/a	103	35	68	77	°C/W
R _{0JC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	4.3	31	n/a	n/a	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.



7.4 Electrical Characteristics: $V_{DD} = 2 V$ for TLC555C, $V_{DD} = 3 V$ for TLC555I

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CON	IDITIONS ⁽¹⁾	MIN	TYP	MAX	UNI	
		0500	TLC555C	0.95	1.33	1.65		
,		25°C	TLC555I	1.6		2.4	V	
/ _{IT}	Threshold voltage	Full searce	TLC555C	0.85		1.75	V	
		Full range	TLC555I	1.5		2.5		
		05%0	TLC555C		10		54	
	Threehold ourrent	25°C	TLC555I		10		рА	
IT Threshold current		TLC555C		75				
	Max	TLC555I		150		рA		
		25%	TLC555C	0.4	0.67	0.95	V	
,	Trigger veltage	25°C	TLC555I	0.71	1	1.29	v	
(TRIG)	Trigger voltage	E. II and an	TLC555C	0.3		1.05	V	
		Full range	TLC555I	0.61		1.39	v	
		25%	TLC555C		10		~ ^	
	Taiaaaa	25°C	TLC555I		10		pA	
I _{I(TRIG)} Trigger current		TLC555C		75				
	Max	TLC555I		150		рА		
V _{I(RESET)} Reset voltage Control voltage (open-circuit) as a	Reset voltage	25°C	TLC555C	0.4	1.1	1.5	V	
			TLC555I	0.4	1.1	1.5		
		Full range	TLC555C	0.3		2	V	
			TLC555I	0.3		1.8		
		TLC555C		66.7%				
	percentage of supply voltage	Max	TLC555I		66.7%			
		I _{OL} = 1 mA, 25°C	TLC555C		0.03	0.2	V	
	Discharge switch on-stage		TLC555I		0.03	0.2		
	voltage		TLC555C			0.25	V	
		I _{OL} = 1 mA, Full range	TLC555I			0.375		
			TLC555C		0.1			
	Discharge switch off-stage	25°C	TLC555I		0.1		nA	
	current		TLC555C		0.5		-	
		Max	TLC555I		120		nA	
			TLC555C	1.5	1.9			
,		I _{OH} = −300 μA, 25°C	TLC555I	2.5	2.85		V	
/ _{он}	High-level output voltage	I _{OH} = -300 μA,	TLC555C	1.5				
		Full range	TLC555I	2.5			V	
			TLC555C		0.07	0.3		
		I _{OL} = 1 mA, 25°C	TLC555I		0.07	0.3	V	
OL	Low-level output voltage	–	TLC555C			0.35		
		$I_{OL} = 1 \text{ mA}$, Full range	TLC555I			0.4	V	
			TLC555C			250		
		25°C	TLC555I			250	μA	
DD	Supply current ⁽²⁾	Full range	TLC555C			400		
			TLC555I			500	μA	

(1) Full range is 0°C to 70°C the for TLC555C, and -40°C to 85°C for the TLC555I. For conditions shown as *Max*, use the appropriate value specified in the *Recommended Operating Conditions* table.

(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.

7.5 Electrical Characteristics: $V_{DD} = 5 V$

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TES	T CONDITIONS ⁽¹⁾	MIN	TYP	MAX	UNIT	
		TLC555C	2.8	3.3	3.8		
	25%	TLC555I	2.8	3.3	3.8	V	
	25 C	TLC555M	2.8	3.3	3.8	v	
Thrashold valtage		TLC555Q	2.8	3.3	3.8		
Threshold voltage		TLC555C	2.7		3.9		
	Eull ronge	TLC555I	2.7		3.9	V	
	Fuil range	TLC555M	2.7		3.9	v	
		TLC555Q	2.7		3.9		
		TLC555C		10			
	25°C	TLC555I		10		pА	
	25 C	TLC555M		10		рА	
Throphold ourrant		TLC555Q		10			
Theshold current		TLC555C		75			
	Mov	TLC555I		150		-	
	wax	TLC555M		5000		pА	
		TLC555Q		5000			
		TLC555C	1.36	1.66	1.96		
	0590	TLC555I	1.36	1.66	1.96		
	25°C	TLC555M	1.36	1.66	1.96	V	
— · · ·		TLC555Q	1.36	1.66	1.96		
Trigger voltage	Full range	TLC555C	1.26		2.06		
		TLC555I	1.26		2.06		
			1.26			V	
			1.26				
	25°C			10			
				10		pА	
				10			
				10			
Trigger current				75		pА	
	Max						
			0.4	1.1	1.5		
	25°C					V	
Reset voltage							
	Full range					V	
			0.0	10	1.5		
	25°C					pА	
Reset current							
	Max					pА	
		I LC0000IVI		5000		·	
_	Threshold voltage Threshold current Trigger voltage Trigger current Reset voltage	25°C Full range 25°C Threshold current 25°C Max Trigger voltage Full range 25°C Max 25°C Max Particular Full range Max Sor Max Sor Max Sor Full range Sor Full range Full range Sor Sor	Hicksic 1100000000000000000000000000000000000	Threshold voltage 25°C TLC555C 2.8 TLC555G 2.8 TLC555G 2.8 TLC555G 2.8 TLC55SG 2.8 TLC55SG 2.7 TLC55SG 1.2 Max TLC55SG TLC55SG 1.36 TLC55SG 1.36 TLC55SG 1.26 TLC55S	Threshold voltage 25°C 1LC656C 2.8 3.3 TLC556M 2.8 3.3 TLC55GQ 2.8 3.3 TLC55GQ 2.7 1 Full range TLC55GI 2.7 TLC55GQ 2.7 1 TLC55GQ 2.7 10 TLC55GQ 1.0 10 TLC55GQ 1.0 10 TLC55SQ 10 10 TLC55GQ 1.36 1.66 TLC55GQ 1.36 1.66 TLC55GQ 1.36 1.66 TLC55GQ 1.36 1.66 TLC55GQ 1.36 1.66	Threshold votage 1LC555C 2.8 3.3 3.8 Tuc555I 2.8 3.3 3.8 Tuc55C 2.8 3.3 3.8 Tuc55C 2.8 3.3 3.8 Tuc55C 2.7 3.9 Tuc55SC 1.0 1.0 Tuc55SC 1.38 1.68 Tuc55SC 1.28 2.06 Tuc55SC 1.28 2.06 Tuc55S	

(1) Full range is 0°C to 70°C the for TLC555C, -40°C to 85°C for the TLC555I, -40°C to 125°C for the TLC555Q, and -55°C to 125°C for the TLC555M. For conditions shown as *Max*, use the appropriate value specified in the *Recommended Operating Conditions* table.



Electrical Characteristics: V_{DD} = 5 V (continued)

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CC	DNDITIONS ⁽¹⁾	MIN	ТҮР	MAX	UNIT
			TLC555C		66.7%		
	Control voltage (open circuit) as a	Max	TLC555I		66.7%		
	percentage of supply voltage	Max	TLC555M		66.7%		
			TLC555Q		66.7%		
			TLC555C		0.14	0.5	
		1 10 1 0500	TLC555I		0.14	0.5	
		I _{OL} = 10 mA, 25°C	TLC555M		0.14	0.5	V
	Discharge switch on-stage		TLC555Q		0.14	0.5	
	voltage		TLC555C			0.6	
		$I_{OI} = 10 \text{ mA},$	TLC555I			0.6	
		I _{OL} = 10 mA, Full range	TLC555M			0.6	V
			TLC555Q			0.6	
			TLC555C		0.1		nA
			TLC555I		0.1		
		25°C	TLC555M		0.1		
Discharge switch off-stage current	Discharge switch off-stage		TLC555Q		0.1		
		Мах	TLC555C		0.5		
			TLC555I		120		nA
			TLC555M		120		
			TLC555Q		120		
		I _{OH} = −1 μA, 25°C	TLC555C	4.1	4.8		
			TLC555I	4.1	4.8		l
			TLC555M	4.1	4.8		V
			TLC555Q	4.1	4.8		
/ _{ОН}	High-level output voltage		TLC555C	4.1			
		I _{ОН} = −1 µА.	TLC555I	4.1			.,
		I _{OH} = −1 μA, Full range	TLC555M	4.1			V
			TLC555Q	4.1			
			TLC555C		0.21	0.4	
			TLC555I		0.21	0.4	
		I _{OL} = 8 mA, 25°C	TLC555M		0.21	0.4	V
			TLC555Q		0.21	0.4	
OL	Low-level output voltage		TLC555C			0.5	
		loi = 8 mA.	TLC555I			0.5	
		I _{OL} = 8 mA, Full range	TLC555M			0.6	V
			TLC555Q			0.6	I

Electrical Characteristics: V_{DD} = 5 V (continued)

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CC	ONDITIONS ⁽¹⁾	MIN	ТҮР	MAX	UNIT
			TLC555C		0.13	0.3	
		$L = 5 m \Lambda 25\%$	TLC555I		0.13	0.3	v
		I _{OL} = 5 mA, 25°C	TLC555M		0.13	0.3	
			TLC555Q		0.13	0.3	
			TLC555C			0.4	
		I _{OL} = 5 mA,	TLC555I			0.4	V
		Full range	TLC555M			0.45	v
v	Low-level output voltage		TLC555Q			0.45	
V _{OL}	Low-level output voltage		TLC555C		0.08	0.3	
		1 3.0 mA 25%	TLC555I		0.08	0.3	V
		I _{OL} = 3.2 mA, 25°C	TLC555M		0.8	0.3	
			TLC555Q		0.8	0.3	
		I _{OL} = 3.2 mA,	TLC555C			0.35	
			TLC555I			0.35	V
		Full range	TLC555M			0.4	v
			TLC555Q			0.4	
			TLC555C		170	350	
		25°C	TLC555I		170	350	
		25.0	TLC555M		170	350	μA
	Supply surrent ⁽²⁾		TLC555Q		170	350	
I _{DD}	Supply current ⁽²⁾		TLC555C			500	
		Full ronge	TLC555I			600	
		Full range	TLC555M			700	μA
			TLC555Q			700	

(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or to TRIG.



7.6 Electrical Characteristics: $V_{DD} = 15 V$

over operating free-air temperature range (unless otherwise noted)

PA	RAMETER	TES	r conditions ⁽¹⁾	MIN	TYP	MAX	UNIT		
			TLC555C	9.45	10	10.55			
		25°C	TLC555I	9.45	10	10.55	V		
		23 0	TLC555M	9.45	10	10.55	v		
/ Throob	old voltage		TLC555Q	9.45	10	10.55			
V _{IT} Thresh	olu voltage		TLC555C	9.35		10.65			
		Full rongo	TLC555I	9.35		10.65	V		
		Full range	TLC555M	9.35		10.65	V		
			TLC555Q	9.35		10.65			
			TLC555C		10				
		25%0	TLC555I		10		~ ^		
		25°C	TLC555M		10		pА		
Thurst	ald assume at		TLC555Q		10				
IT Thresh	old current		TLC555C		75				
			TLC555I		150				
		Max	TLC555M		5000		pА		
			TLC555Q		5000				
			TLC555C	4.65	5	5.35			
			TLC555I	4.65	5	5.35	V		
		25°C	TLC555M	4.65	5	5.35			
V _{I(TRIG)} Trigger voltage		TLC555Q	4.65	5	5.35				
		TLC555C	4.55		5.45				
		TLC555I	4.55		5.45				
		Full range	TLC555M	4.55		5.45	V		
			TLC555Q	4.55		5.45			
		TLC555C	1.00	10	0.10				
		TLC5551		10					
		25°C	TLC555M		10		pА		
			TLC555Q		10				
I(TRIG) Trigger	current	Max	TLC555C		75		рА		
			TLC555I		150				
			TLC555M		5000				
			TLC555Q		5000		1		
			TLC555C	0.4	1.1	1.5			
			TLC555I	0.4	1.1	1.5			
		25°C	TLC555M	0.4	1.1	1.5	V		
			TLC555Q	0.4	1.1	1.5			
V _{I(RESET)} Reset v	voltage		TLC555C	0.3	1.1	1.3			
			TLC555I	0.3		1.8			
		Full range	TLC555M	0.3		1.8	V		
			TLC555Q	0.3		1.8			
				0.3	10	1.0			
			TLC555C TLC555I		10 10				
		25°C					pА		
			TLC555M		10				
(RESET) Reset of	current		TLC555Q		10				
			TLC555C		75				
		Max	TLC555I		150		pА		
			TLC555M		5000				
			TLC555Q		5000				

(1) Full range is 0°C to 70°C for TLC555C, -40°C to 85°C for TLC555I, -40°C to 125°C for the TLC555Q, and -55°C to 125°C for TLC555M. For conditions shown as *Max*, use the appropriate value specified in the *Recommended Operating Conditions* table.

Electrical Characteristics: V_{DD} = 15 V (continued)

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CO	NDITIONS ⁽¹⁾	MIN	TYP	MAX	UNI
			TLC555C		66.7%		
	Control voltage (open circuit) as a	Max	TLC555I		66.7%		
percentage of supply voltage	percentage of supply voltage	IVIAX	TLC555M		66.7%		
			TLC555Q		66.7%		
			TLC555C		0.77	1.7	V
		$1 - 100 \text{ m} = 35^{\circ}\text{C}$	TLC555I		0.77	1.7	
		I _{OL} = 100 mA, 25°C	TLC555M		0.77	1.7	
	Discharge switch on-stage		TLC555Q		0.77	1.7	
	voltage		TLC555C			1.8	
		I _{OL} = 100 mA,	TLC555I			1.8	.,
		Full range	TLC555M			1.8	V
			TLC555Q			1.8	
			TLC555C		0.1		
			TLC555I		0.1		
		25°C	TLC555M		0.1		nA
	Discharge switch off-stage		TLC555Q		0.1		
	current		TLC555C		0.5		nA
			TLC555I		120		
		Max	TLC555M		120		
			TLC555Q		120		
		I _{OH} = −10 mA, 25°C	TLC555C	12.5	14.2		- V
			TLC555I	12.5	14.2		
			TLC555M	12.5	14.2		
			TLC555Q	12.5	14.2		
		I _{OH} = −10 mA, Full range	TLC555C	12.5			- V
			TLC555I	12.5			
			TLC555M	12.5			
			TLC555Q	12.5			
			TLC555C	13.5	14.6		
			TLC555I	13.5	14.6		
		I _{OH} = -5 mA, 25°C	TLC555M	13.5	14.6		V
			TLC555Q	13.5	14.6		
н	High-level output voltage		TLC555C	13.5	14.0		
		L	TLC555I	13.5			
		I _{OH} = -5 mA, Full range	TLC555M	13.5			V
		, č	TLC555Q	13.5			
			TLC555C	13.5	14.9		
			TLC555I	14.2	14.9		
		I _{OH} = −1 mA, 25°C	TLC555M	14.2	14.9		V
							-
			TLC555Q	14.2	14.9		
			TLC555C	14.2			
		I _{OH} = −1 mA, Full range	TLC555I	14.2			V
		i uli ialiye	TLC555M	14.2			
			TLC555Q	14.2			



Electrical Characteristics: V_{DD} = 15 V (continued)

over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CO	NDITIONS ⁽¹⁾	MIN	ТҮР	MAX	UNIT
			TLC555C		1.28	3.2	
		100 0 05%0	TLC555I		1.28	3.2	V
		I _{OL} = 100 mA, 25°C	TLC555M		1.28	3.2	
			TLC555Q		1.28	3.2	
			TLC555C			3.6	
		I _{OL} = 100 mA,	TLC555I			3.7	V
		Full range	TLC555M			3.8	v
			TLC555Q			3.8	
			TLC555C		0.63	1	
		50 4 05%0	TLC555I		0.63	1	N/
		I _{OL} = 50 mA, 25°C	TLC555M		0.63	1	V
			TLC555Q		0.63	1	
V _{OL}	Low-level output voltage	ge I _{OL} = 50 mA, Full range	TLC555C			1.3	V
			TLC555I			1.4	
			TLC555M			1.5	
			TLC555Q			1.5	
			TLC555C		0.12	0.3	V
		I _{OL} = 10 mA, 25°C	TLC555I		0.12	0.3	
		$1_{OL} = 10$ mA, 25 C	TLC555M		0.12	0.3	
			TLC555Q		0.12	0.3	
			TLC555C			0.4	
		I _{OL} = 10 mA,	TLC555I			0.4	
		Full range	TLC555M			0.45	V
			TLC555Q			0.45	
			TLC555C		360	600	
		0590	TLC555I		360	600	
		25°C	TLC555M		360	600	μA
	Supply current ⁽²⁾		TLC555Q		360	600	
I _{DD}			TLC555C			800	
		Full rongs	TLC555I			900	
		Full range	TLC555M			1000	μA
			TLC555Q			1000	

(2) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

STRUMENTS

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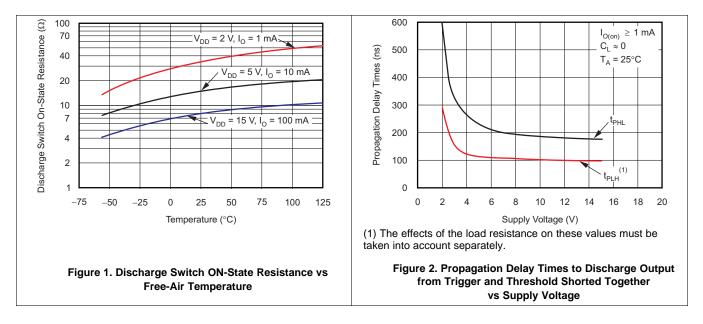
7.7 Electrical Characteristics: $V_{DD} = 5 V$

At $T_A = 25^{\circ}$ C, over operating free-air temperature range (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V _{IT}	Threshold voltage		2.8	3.3	3.8	V
I _{IT}	Threshold current			10		pА
V _{I(TRIG)}	Trigger voltage		1.36	1.66	1.96	V
I _{I(TRIG)}	Trigger current			10		pА
V _{I(RESET)}	Reset voltage		0.4	1.1	1.5	V
II(RESET)	Reset current			10		pА
	Control voltage (open circuit) as a percentage of supply voltage			66.7%		
	Discharge switch on-stage voltage	I _{OL} = 10 mA		0.14	0.5	v
	Discharge switch off-stage current			0.1		nA
V _{OH}	High-level output voltage	$I_{OH} = -1 \text{ mA}$	4.1	4.8		V
		I _{OL} = 8 mA		0.21	0.4	V
V _{OL}	Low-level output voltage	$I_{OL} = 5 \text{ mA}$		0.13	0.3	V
		I _{OL} = 3.2 mA		0.08	0.3	V
I _{DD}	Supply current ⁽¹⁾			170	350	μA

(1) These values apply for the expected operating configurations in which THRES is connected directly to DISCH or TRIG.

7.8 Typical Characteristics



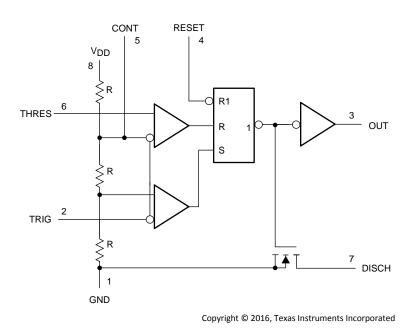


8 Detailed Description

8.1 Overview

The TLC555 is a precision timing device used for general-purpose timing applications up to 2.1 MHz.

8.2 Functional Block Diagram



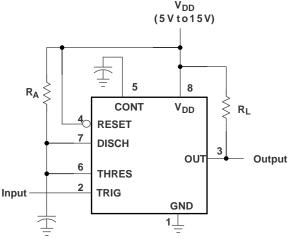
Pin numbers are for all packages except the FK package. RESET can override TRIG, which can override THRES.

8.3 Feature Description

8.3.1 Monostable Operation

For monostable operation, any of these timers can be connected as shown in Figure 3. If the output is low, application of a negative-going pulse to the trigger (TRIG) sets the flip-flop (\overline{Q} goes low), drives the output high, and turns off Q1. Capacitor C then is charged through R_A until the voltage across the capacitor reaches the threshold voltage of the threshold (THRES) input. If TRIG has returned to a high level, the output of the threshold comparator resets the flip-flop (\overline{Q} goes high), drives the output low, and discharges C through Q1.

Feature Description (continued)

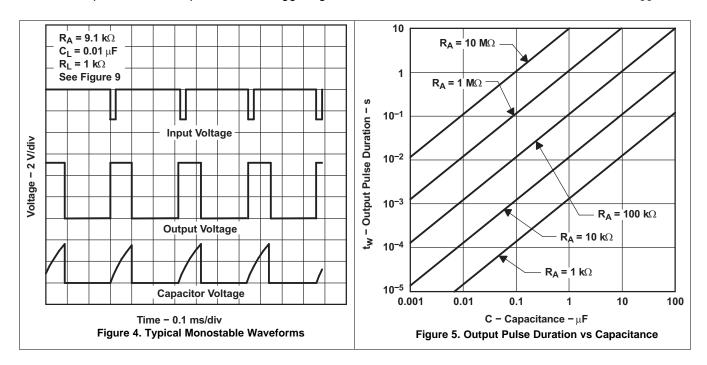


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Figure 3. Circuit for Monostable Operation

Monostable operation is initiated when TRIG voltage falls below the trigger threshold. Once initiated, the sequence ends only if TRIG is high for at least 10 μ s before the end of the timing interval. When the trigger is grounded, the comparator storage time can be as long as 10 μ s, which limits the minimum monostable pulse width to 10 μ s. Because of the threshold level and saturation voltage of Q1, the output pulse duration is approximately t_w = 1.1R_AC. Figure 4 is a plot of the time constant for various values of R_A and C. The threshold levels and charge rates both are directly proportional to the supply voltage, V_{CC}. The timing interval is, therefore, independent of the supply voltage, so long as the supply voltage is constant during the time interval.

Applying a negative-going trigger pulse simultaneously to RESET and TRIG during the timing interval discharges C and reinitiates the cycle, commencing on the positive edge of the reset pulse. The output is held low as long as the reset pulse is low. To prevent false triggering, when RESET is not used it must be connected to V_{CC}.





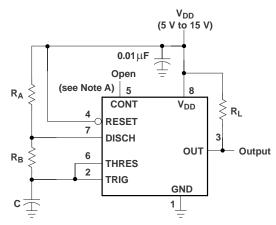
Feature Description (continued)

8.3.2 Astable Operation

As shown in Figure 6, adding a second resistor, R_B, to the circuit of Figure 3 and connecting the trigger input to the threshold input causes the timer to self-trigger and run as a multi-vibrator. The capacitor C charges through R_A and R_B and then discharges through R_B only. Therefore, the duty cycle is controlled by the values of R_A and R_B.

This astable connection results in capacitor C charging and discharging between the threshold-voltage level (≈ 0.67 × V_{CC}) and the trigger-voltage level (≈ 0.33 × V_{CC}). As in the monostable circuit, charge and discharge times (and, therefore, the frequency and duty cycle) are independent of the supply voltage.

Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.



NOTE A: Decoupling CONT voltage to ground with a capacitor can improve operation. This should be evaluated for individual applications.

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 $R_A = 5 k\Omega$ $\mathbf{R}_{\mathbf{L}} = \mathbf{1} \mathbf{k} \Omega$ $R_B = 3 k\Omega$ See Figure 12 $C = 0.15 \,\mu F$ Voltage – 1 V/div ιн **Output Voltage** tL **Capacitor Voltage**

Time - 0.5 ms/div

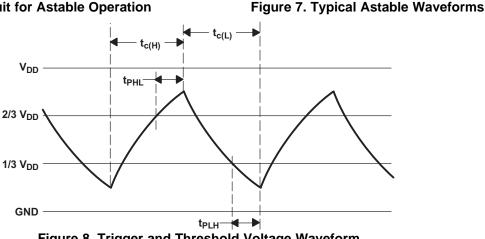


Figure 8. Trigger and Threshold Voltage Waveform

Figure 7 shows typical waveforms generated during astable operation. The output high-level duration t_H and lowlevel duration t₁ can be calculated as follows:

$t_{\rm H} = 0.693 \left({\rm R}_{\rm A} + {\rm R}_{\rm B} \right) {\rm C}$	(1)
$t_{L} = 0.693(R_{B})C$	(2)
Other useful relationships are shown below:	
$period = t_{H} + t_{L} = 0.693 (R_{A} + 2R_{B})C$	(3)

Feature Description (continued)

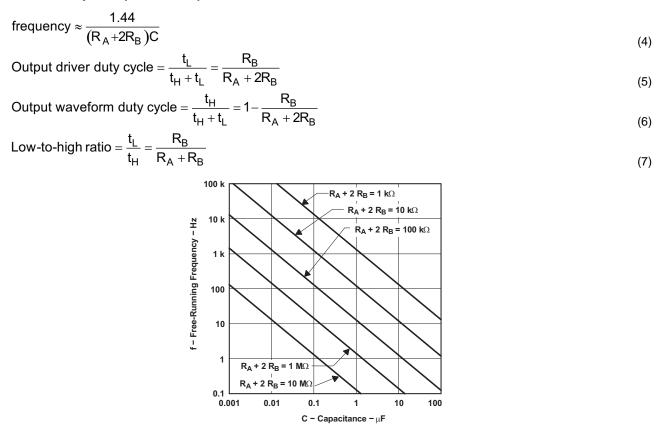


Figure 9. Free-Running Frequency

8.3.3 Frequency Divider

By adjusting the length of the timing cycle, the basic circuit of Figure 6 can be made to operate as a frequency divider. Figure 10 shows a divide-by-three circuit that makes use of the fact that re-triggering cannot occur during the timing cycle.

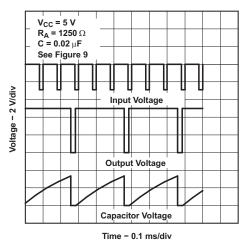


Figure 10. Divide-by-Three Circuit Waveforms



8.4 Device Functional Modes

Table 1 shows the device functional modes.

RESET VOLTAGE ⁽¹⁾	TRIGGER VOLTAGE ⁽¹⁾	THRESHOLD VOLTAGE ⁽¹⁾	OUTPUT	DISCHARGE SWITCH	
<min< td=""><td>Irrelevant</td><td>Irrelevant</td><td>L</td><td>On</td></min<>	Irrelevant	Irrelevant	L	On	
>MAX	<min< td=""><td>Irrelevant</td><td>н</td><td>Off</td></min<>	Irrelevant	н	Off	
>MAX	>MAX	>MAX	L	On	
>MAX	>MAX	<min< td=""><td colspan="3">As previously established</td></min<>	As previously established		

Table 1. Function Table

(1) For conditions shown as MIN or MAX, use the appropriate value specified under *Electrical Characteristics:* $V_{DD} = 5 V$.

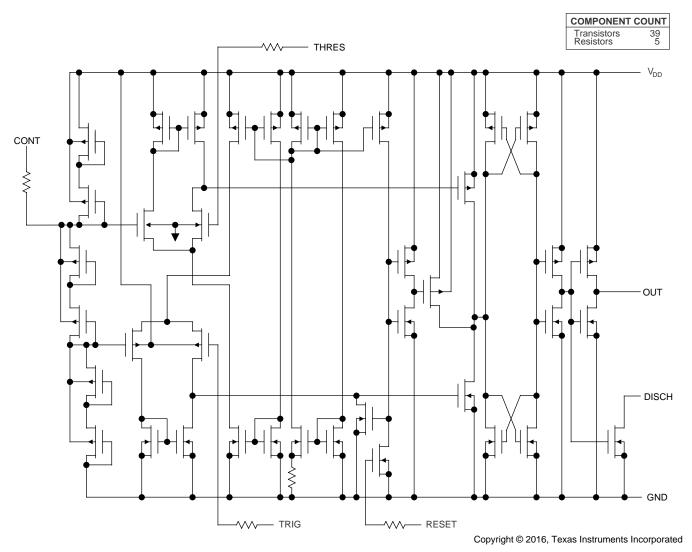


Figure 11. Equivalent Schematic (Each Channel)

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9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

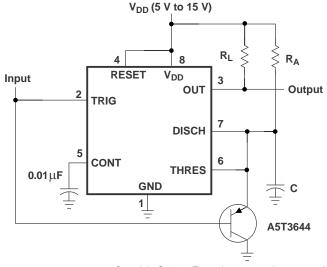
9.1 Application Information

The TLC555 timer device uses resistor and capacitor charging delay to provide a programmable time delay or operating frequency. The *Typical Applications* section presents a simplified discussion of the design process.

9.2 Typical Applications

9.2.1 Missing-Pulse Detector

The circuit shown in Figure 12 can be used to detect a missing pulse or abnormally long spacing between consecutive pulses in a train of pulses. The timing interval of the monostable circuit is re-triggered continuously by the input pulse train as long as the pulse spacing is less than the timing interval. A longer pulse spacing, missing pulse, or terminated pulse train permits the timing interval to be completed, thereby generating an output pulse as shown in Figure 13.



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Figure 12. Circuit for Missing-Pulse Detector

9.2.1.1 Design Requirements

Input fault (missing pulses) must be input high. An input stuck low cannot be detected because the timing capacitor (C) remains discharged.

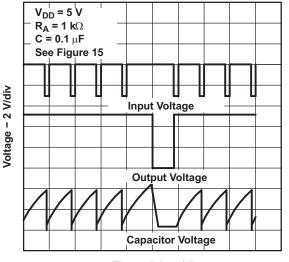
9.2.1.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C > [maximum normal input high time]$. R_L improves V_{OH} , but it is not required for TTL compatibility.



Typical Applications (continued)

9.2.1.3 Application Curve

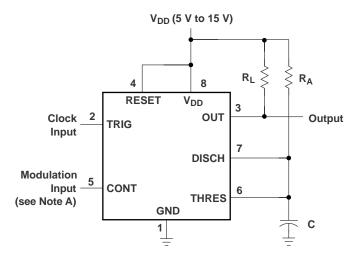


Time - 0.1 ms/div



9.2.2 Pulse-Width Modulation

The operation of the timer can be modified by modulating the internal threshold and trigger voltages, which is accomplished by applying an external voltage (or current) to CONT. Figure 14 shows a circuit for pulse-width modulation. A continuous input pulse train triggers the monostable circuit, and a control signal modulates the threshold voltage. Figure 15 shows the resulting output pulse-width modulation. While a sine-wave modulation signal is shown, any wave shape could be used.



NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

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The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, consider the effects of modulation source voltage and impedance on the bias of the timer.

Figure 14. Circuit for Pulse-Width Modulation



Typical Applications (continued)

9.2.2.1 Design Requirements

The clock input must have V_{OL} and V_{OH} levels that are less than and greater than 1/3 V_{DD} , respectively. Modulation input can vary from ground to V_{DD} . The application must be tolerant of a nonlinear transfer function; the relationship between modulation input and pulse width is not linear because the capacitor charge is RC based with an negative exponential curve.

9.2.2.2 Detailed Design Procedure

Choose R_A and C so that $R_A \times C = 1/4$ [clock input period]. R_L improves V_{OH} , but it is not required for TTL compatibility.

9.2.2.3 Application Curve

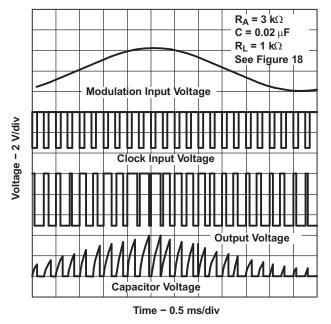


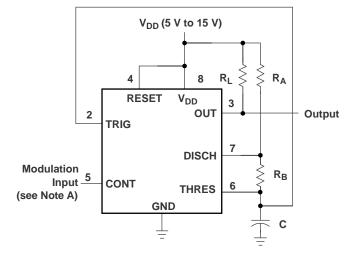
Figure 15. Pulse-Width-Modulation Waveforms

9.2.3 Pulse-Position Modulation

As shown in Figure 16, any of these timers can be used as a pulse-position modulator. This application modulates the threshold voltage and thereby the time delay of a free-running oscillator. Figure 17 shows a triangular-wave modulation signal for such a circuit; however, any wave shape could be used.



Typical Applications (continued)



NOTE A: The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, the effects of modulation source voltage and impedance on the bias of the timer should be considered.

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The modulating signal can be direct or capacitively coupled to CONT. For direct coupling, consider the effects of modulation source voltage and impedance on the bias of the timer.

Figure 16. Circuit for Pulse-Position Modulation



Typical Applications (continued)

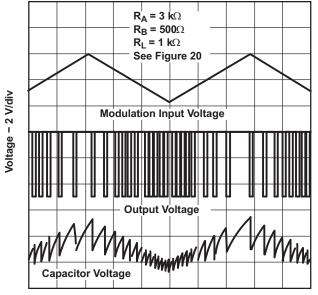
9.2.3.1 Design Requirements

Both DC- and AC-coupled modulation input changes the upper and lower voltage thresholds for the timing capacitor. Both frequency and duty cycle vary with the modulation voltage.

9.2.3.2 Detailed Design Procedure

The nominal output frequency and duty cycle can be determined using formulas in *Astable Operation*. R_L improves V_{OH}, but it is not required for TTL compatibility.

9.2.3.3 Application Curve



Time - 0.1 ms/div

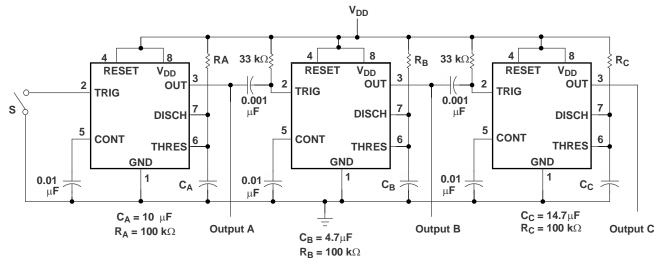
Figure 17. Pulse-Position-Modulation Waveforms

9.2.4 Sequential Timer

Many applications, such as computers, require signals for initializing conditions during start-up. Other applications, such as test equipment, require activation of test signals in sequence. These timing circuits can be connected to provide such sequential control. The timers can be used in various combinations of astable or monostable circuit connections, with or without modulation, for extremely flexible waveform control. Figure 18 shows a sequencer circuit with possible applications in many systems, and Figure 19 shows the output waveforms.



Typical Applications (continued)



NOTE A: S closes momentarily at t = 0.

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S closes momentarily at t = 0.

Figure 18. Sequential Timer Circuit

9.2.4.1 Design Requirements

The sequential timer application chains together multiple monostable timers. The joining components are the 33-k Ω resistors and 0.001-µF capacitors. The output high to low edge passes a 10-µs start pulse to the next monostable.

9.2.4.2 Detailed Design Procedure

The timing resistors and capacitors can be chosen using this formula: $t_w = 1.1 \times R \times C$.



Typical Applications (continued)

9.2.4.3 Application Curve

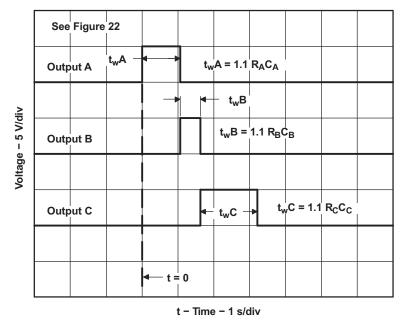


Figure 19. Sequential Timer Waveforms

10 Power Supply Recommendations

The TLC555 requires a voltage supply within 2 V to 15 V. Adequate power supply bypassing is necessary to protect associated circuitry. Minimum recommended is $0.1-\mu F$ ceramic in parallel with $1-\mu F$ electrolytic. Place the bypass capacitors as close as possible to the TLC555 and minimize the trace length.



11 Layout

11.1 Layout Guidelines

Standard PCB rules apply to routing the TLC555. The $0.1-\mu$ F ceramic capacitor in parallel with a $1-\mu$ F electrolytic capacitor must be as close as possible to the TLC555. The capacitor used for the time delay must also be placed as close to the discharge pin. A ground plane on the bottom layer can be used to provide better noise immunity and signal integrity.

Figure 20 is the basic layout for various applications.

- C1—based on time delay calculations
- C2-0.01-µF bypass capacitor for control voltage pin
- C3—0.1-μF bypass ceramic capacitor
- C4—1-μF electrolytic bypass capacitor
- R1—based on time-delay calculations

11.2 Layout Example

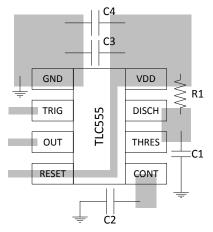


Figure 20. Layout Example

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12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — TI Glossary.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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