

## INA12x Precision, Low Power Instrumentation Amplifiers

### 1 Features

- Low Offset Voltage: 50  $\mu\text{V}$  Maximum
- Low Drift: 0.5  $\mu\text{V}/^\circ\text{C}$  Maximum
- Low Input Bias Current: 5 nA Maximum
- High CMR: 120 dB minimum
- Inputs Protected to  $\pm 40\text{ V}$
- Wide Supply Range:  $\pm 2.25\text{ V}$  to  $\pm 18\text{ V}$
- Low Quiescent Current: 700  $\mu\text{A}$
- 8-PIN Plastic Dip, SO-8

### 2 Applications

- Bridge Amplifier
- Thermocouple Amplifier
- RTD Sensor Amplifier
- Medical Instrumentation
- Data Acquisition

### 3 Description

The INA128 and INA129 are low-power, general purpose instrumentation amplifiers offering excellent accuracy. The versatile 3-op amp design and small size make these amplifiers ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain (200 kHz at  $G = 100$ ).

A single external resistor sets any gain from 1 to 10,000. The INA128 provides an industry-standard gain equation; the INA129 gain equation is compatible with the AD620.

The INA12x is laser-trimmed for very low offset voltage (50  $\mu\text{V}$ ), drift (0.5  $\mu\text{V}/^\circ\text{C}$ ) and high common-mode rejection (120 dB at  $G \geq 100$ ). The INA12x operates with power supplies as low as  $\pm 2.25\text{ V}$ , and quiescent current is only 700  $\mu\text{A}$ , ideal for battery-operated systems. Internal input protection can withstand up to  $\pm 40\text{ V}$  without damage.

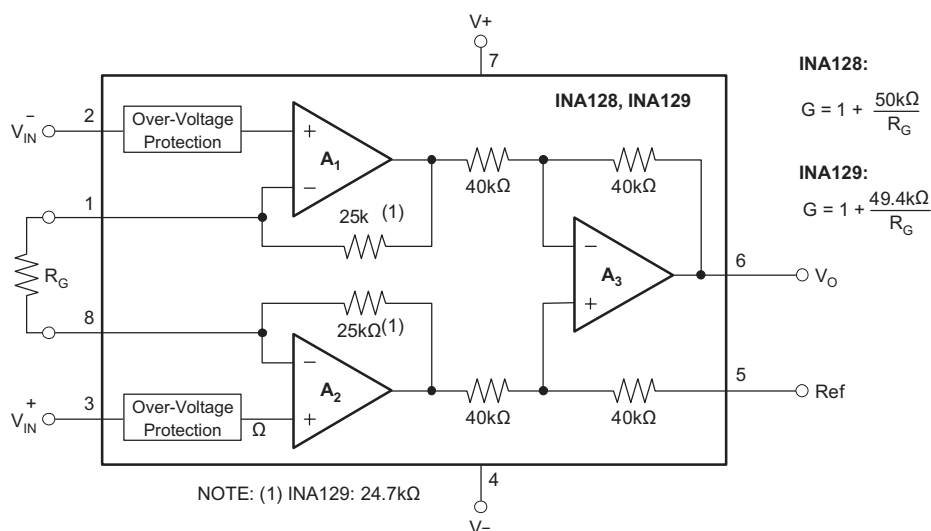
The INA12x is available in 8-pin plastic DIP and SO-8 surface-mount packages, specified for the  $-40^\circ\text{C}$  to  $85^\circ\text{C}$  temperature range. The INA128 is also available in a dual configuration, the INA2128.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
INA128	SOIC (8)	3.91 mm x 4.9 mm
INA129	PDIP (8)	6.35 mm x 9.81 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

#### Simplified Schematic



## Table of Contents

<b>1 Features</b> .....	<b>1</b>	7.4 Device Functional Modes.....	<b>11</b>
<b>2 Applications</b> .....	<b>1</b>	<b>8 Application and Implementation</b> .....	<b>13</b>
<b>3 Description</b> .....	<b>1</b>	8.1 Application Information.....	<b>13</b>
<b>4 Revision History</b> .....	<b>2</b>	8.2 Typical Application .....	<b>13</b>
<b>5 Pin Configuration and Functions</b> .....	<b>3</b>	<b>9 Power Supply Recommendations</b> .....	<b>16</b>
<b>6 Specifications</b> .....	<b>3</b>	9.1 Low Voltage Operation .....	<b>16</b>
6.1 Absolute Maximum Ratings .....	<b>3</b>	<b>10 Layout</b> .....	<b>18</b>
6.2 ESD Ratings.....	<b>3</b>	10.1 Layout Guidelines .....	<b>18</b>
6.3 Recommended Operating Conditions .....	<b>4</b>	10.2 Layout Example .....	<b>19</b>
6.4 Thermal Information .....	<b>4</b>	<b>11 Device and Documentation Support</b> .....	<b>20</b>
6.5 Electrical Characteristics.....	<b>4</b>	11.1 Community Resources.....	<b>20</b>
6.6 Typical Characteristics.....	<b>7</b>	11.2 Related Links .....	<b>20</b>
<b>7 Detailed Description</b> .....	<b>11</b>	11.3 Trademarks .....	<b>20</b>
7.1 Overview .....	<b>11</b>	11.4 Electrostatic Discharge Caution.....	<b>20</b>
7.2 Functional Block Diagram .....	<b>11</b>	11.5 Glossary .....	<b>20</b>
7.3 Feature Description.....	<b>11</b>	<b>12 Mechanical, Packaging, and Orderable Information</b> .....	<b>20</b>

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

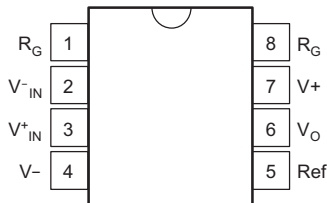
### Changes from Revision B (February 2005) to Revision C

Page

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. .... **1**

## 5 Pin Configuration and Functions

**D and P Packages  
8 Pin SOIC and PDIP  
Top View**



**Pin Functions**

PIN		I/O	DESCRIPTION
NAME	NO.		
REF	5	I	Reference input. This pin must be driven by low impedance or connected to ground.
R <sub>G</sub>	1,8	—	Gain setting pin. For gains greater than 1, place a gain resistor between pin 1 and pin 8.
V <sup>-</sup>	4	—	Negative supply
V <sup>+</sup>	7	—	Positive supply
V <sub>IN-</sub>	2	I	Negative input
V <sub>IN+</sub>	3	I	Positive input
V <sub>O</sub>	6	I	Output

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

	MIN	MAX	UNIT
Supply voltage		±18	V
Analog input voltage		±40	V
Output short circuit (to ground)		continuous	
Operating temperature	-40	125	°C
Junction temperature		150	°C
Lead temperature (soldering, 10s)		300	°C
T <sub>stg</sub> Storage temperature	-55	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

		VALUE	UNIT
V <sub>(ESD)</sub> Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	±2000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	±50	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
V power supply	±2.25	±15	±18	V
Input common-mode voltage range for $V_O = 0$	V – +2 V		V + –2 V	
T <sub>A</sub> operating temperature INA128-HT	–55		175	°C
T <sub>A</sub> operating temperature INA129-HT	–55		210	°C

### 6.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>		INA12x		UNIT
		D (SOIC)	P (PDIP)	
		8 PINS	8 PINS	
R <sub>θJA</sub>	Junction-to-ambient thermal resistance	110	46.1	°C/W
R <sub>θJC(top)</sub>	Junction-to-case (top) thermal resistance	57	34.1	°C/W
R <sub>θJB</sub>	Junction-to-board thermal resistance	54	23.4	°C/W
Ψ <sub>JT</sub>	Junction-to-top characterization parameter	11	11.3	°C/W
Ψ <sub>JB</sub>	Junction-to-board characterization parameter	53	23.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, [SPRA953](#).

### 6.5 Electrical Characteristics

 At T<sub>A</sub> = 25°C, V<sub>S</sub> = ±15 V, R<sub>L</sub> = 10 kΩ, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
<b>INPUT</b>							
Offset Voltage, RTI	Initial	T <sub>A</sub> = 25°C	INA128P, U INA129P, U	±10±100/G	±50±500/G		μV
			INA128PA, UA INA129PA, UA	±25±100/G	±125±1000/G		
	vs Temperature	T <sub>A</sub> = T <sub>MIN</sub> to T <sub>MAX</sub>	INA128P, U INA129P, U	±0.2±2/G	±0.5±0/G		μV/°C
			INA128PA, UA INA129PA, UA	±0.2±5/G	±1±20/G		
	vs Power Supply	V <sub>S</sub> = ±2.25 V to ±18 V	INA128P, U INA129P, U	±0.2±20/G	±1±100/G		μV/V
			INA128PA, UA INA129PA, UA		±2±200/G		
	Long-Term Stability			±0.1±3/g			μV/mo
Impedance	Differential			10 <sup>10</sup>    2			Ω    pF
	Common-Mode			10 <sup>11</sup>    9			
Common-Mode Voltage Range <sup>(1)</sup>		V <sub>O</sub> = 0 V		(V+) - 2	(V+) - 1.4		V
				(V-) + 2	(V-) + 1.7		
Safe Input Voltage						±40	V

(1) Input common-mode range varies with output voltage - see [Typical Characteristics](#).

**Electrical Characteristics (continued)**

At TA = 25°C, VS = ±15 V, RL = 10 kΩ, unless otherwise noted.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT	
Common-Mode Rejection		G = 1	INA128P, U INA129P, U	80	86		dB	
			INA128PA, UA INA129PA, UA	73				
		G = 10	INA128P, U INA129P, U	100	106			
			INA128PA, UA INA129PA, UA	93				
		G = 100	INA128P, U INA129P, U	120	125			
			INA128PA, UA INA129PA, UA	110				
		G = 1000	INA128P, U INA129P, U	120	130			
			INA128PA, UA INA129PA, UA	110				
Bias Current		INA128P, U INA129P, U			±2	±5	nA	
		INA128PA, UA INA129PA, UA				±10		
Bias Current vs Temperature					±30		pA/°C	
Offset Current		INA128P, U INA129P, U			±1	±5	nA	
		INA128PA, UA INA129PA, UA				±10		
Offset Current vs Temperature					±30		pA/°C	
Noise Voltage, RTI	f = 10 Hz	G = 1000, RS = 0Ω			10		nV/√Hz	
	f = 100 Hz				8			
	f = 1 kHz				8			
	fB = 0.1 Hz to 10 Hz				0.2		μVPP	
Noise Current	f = 10 Hz				0.9		pA/√Hz	
	f = 1 kHz				0.3			
	FB = 0.1 Hz to 10 Hz				30		pAPP	
<b>GAIN</b>								
Gain Equation	INA128			1 + (50 kΩ/RG)			V/V	
	INA129			1 + (49.4 kΩ/RG)				
Range of Gain				1		10000	V/V	
Gain Error	G = 1		INA128P, U INA129P, U		±0.01%	±0.024%		
			INA128PA, UA INA129PA, UA			±0.01%		
	G = 10		INA128P, U INA129P, U		±0.02%	±0.4%		
			INA128PA, UA INA129PA, UA			±0.5%		
	G = 100		INA128P, U INA129P, U		±0.05%	±0.5%		
			INA128PA, UA INA129PA, UA			±0.7%		
	G = 1000		INA128P, U INA129P, U		±0.5%	±1%		
			INA128PA, UA INA129PA, UA			±2%		

**INA128, INA129**

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**Electrical Characteristics (continued)**

At TA = 25°C, VS = ±15 V, RL = 10 kΩ, unless otherwise noted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Gain vs Temperature <sup>(2)</sup>	G = 1			±1	±10	ppm/°C
	50-kΩ (or 49.4-kΩ) Resistance <sup>(2)(3)</sup>			±25	±100	
Nonlinearity	VO = ±13.6 V, G = 1	INA128P, U INA129P, U		±0.0001	±0.001	% of FSR
		INA128PA, UA INA129PA, UA			±0.002	
	G = 10	INA128P, U INA129P, U		±0.0003	±0.002	
		INA128PA, UA INA129PA, UA			±0.004	
	G = 100	INA128P, U INA129P, U		±0.0005	±0.002	
		INA128PA, UA INA129PA, UA			±0.004	
G = 1000			±0.001			
<b>(4) OUTPUT</b>						
Voltage	Positive	RL = 10 kΩ	(V+) - 1.4	(V+) - 0.9		V
	Negative	RL = 10 kΩ	(V-) + 1.4	(V-) + 0.8		
Load Capacitance Stability				1000		pF
Short Circuit Current				6/-15		mA
<b>FREQUENCY RESPONSE</b>						
Bandwidth, -3 dB	G = 1			1.3		MHz
	G = 10			700		kHz
	G = 100			200		
	G = 1000			20		
Slew Rate	VO = ±10 V, G = 10			4		V/μs
Settling Time, 0.01%	G = 1			7		μs
	G = 10			7		
	G = 100			9		
	G = 1000			80		
Overload Recovery	50% Overdrive			4		μs
<b>POWER SUPPLY</b>						
Voltage Range			±2.25	±15	±18	V
Current, Total	VIN = 0 V			±700	±750	μA
<b>TEMPERATURE RANGE</b>						
Specification			-40		85	°C
Operating			-40		125	°C

(2) Specified by wafer test.

(3) Temperature coefficient of the 50 kΩ (or 49.4 kΩ) term in the gain equation.

(4) Nonlinearity measurements in G = 1000 are dominated by noise. Typical non-linearity is ±0.001%.

## 6.6 Typical Characteristics

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , unless otherwise noted.

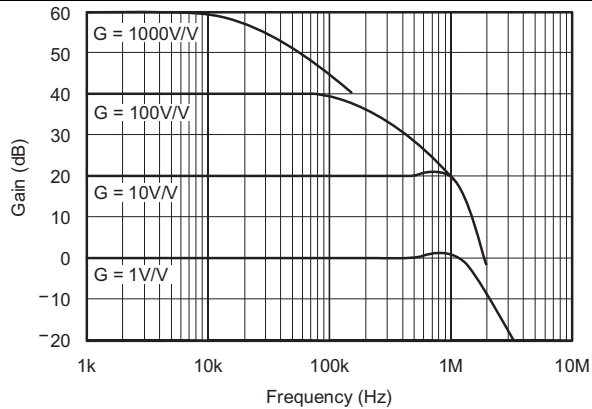


Figure 1. Gain vs Frequency

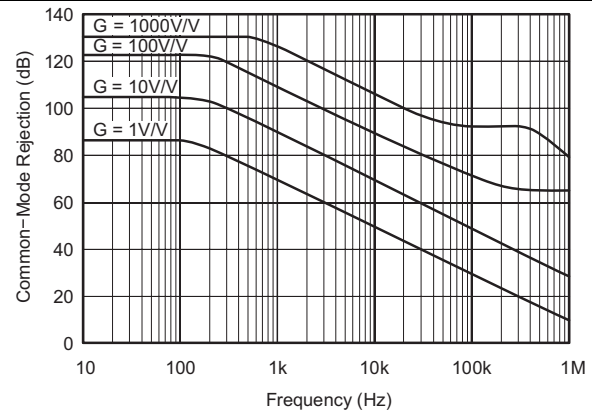


Figure 2. Common-Mode Rejection vs Frequency

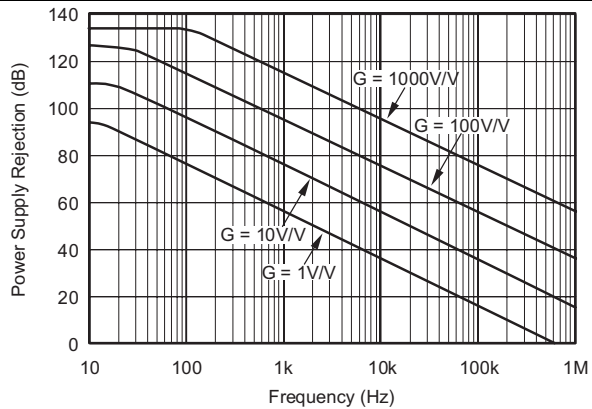


Figure 3. Positive Power Supply Rejection vs Frequency

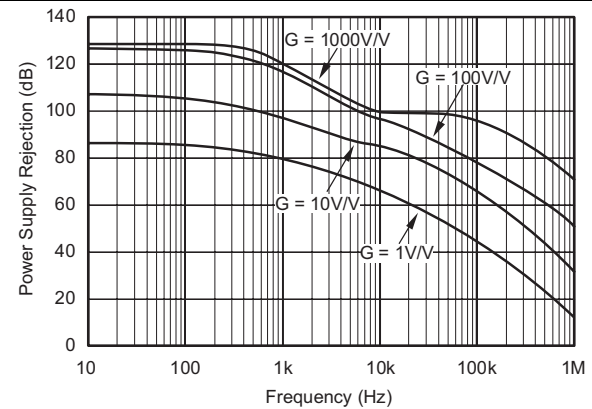


Figure 4. Negative Power Supply Rejection vs Frequency

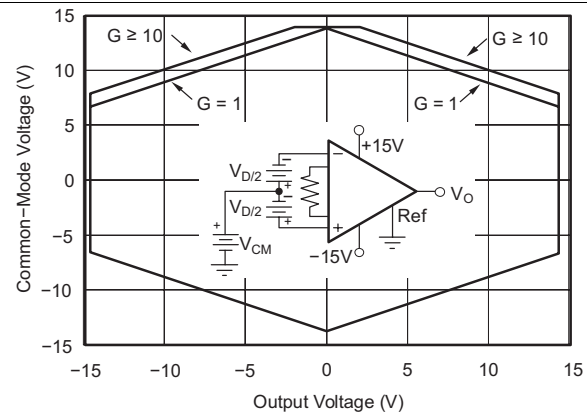


Figure 5. Input Common-Mode Range vs Output Voltage,  $V_S = \pm 15\text{ V}$

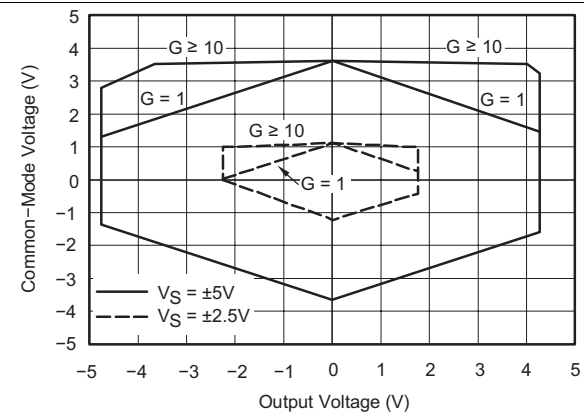
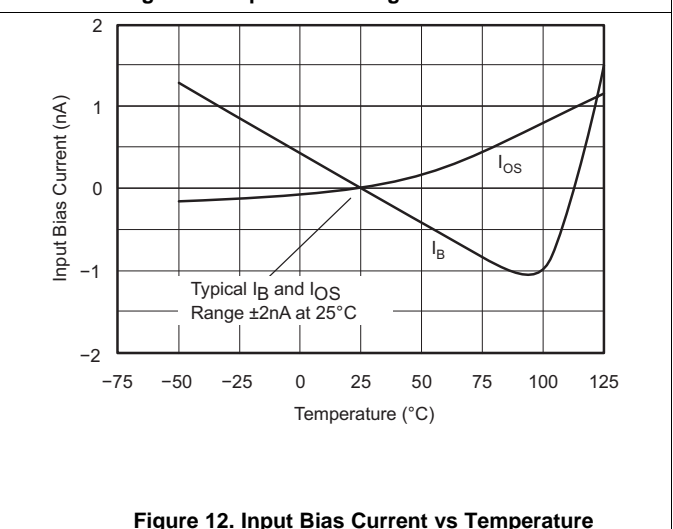
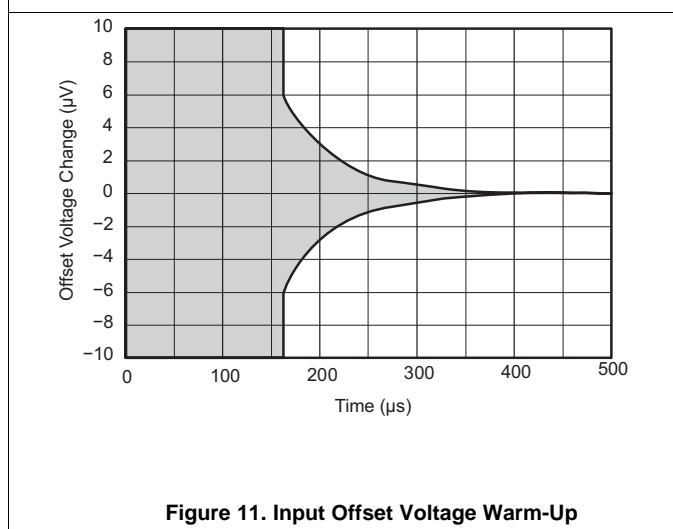
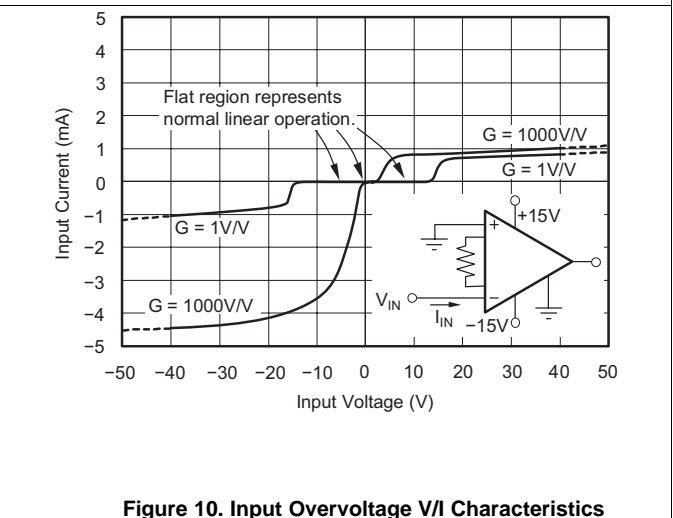
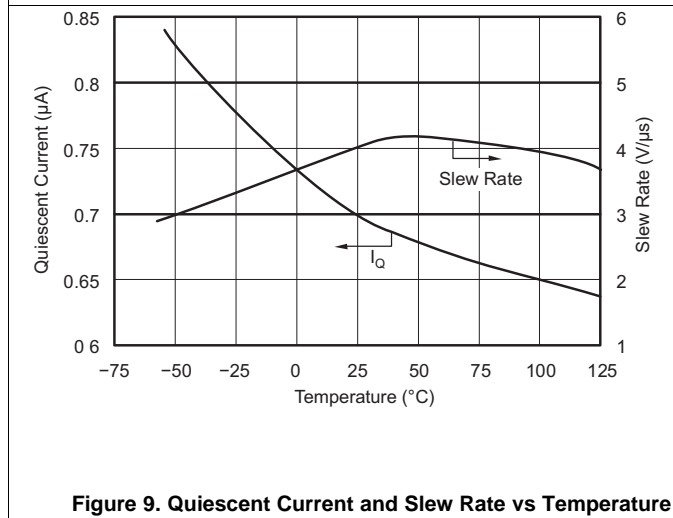
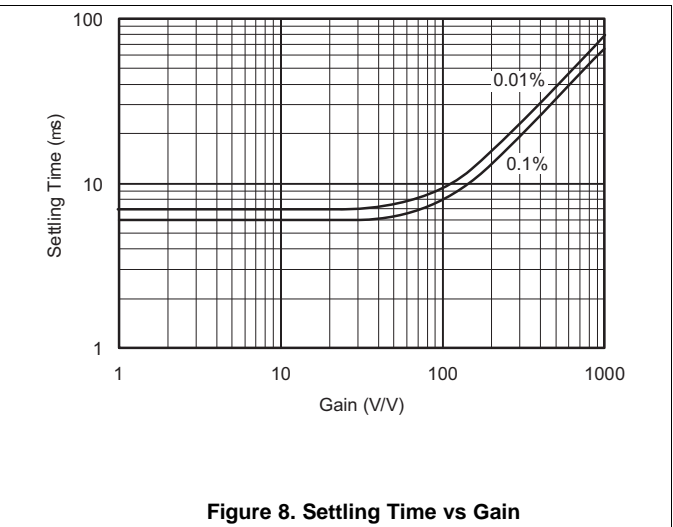
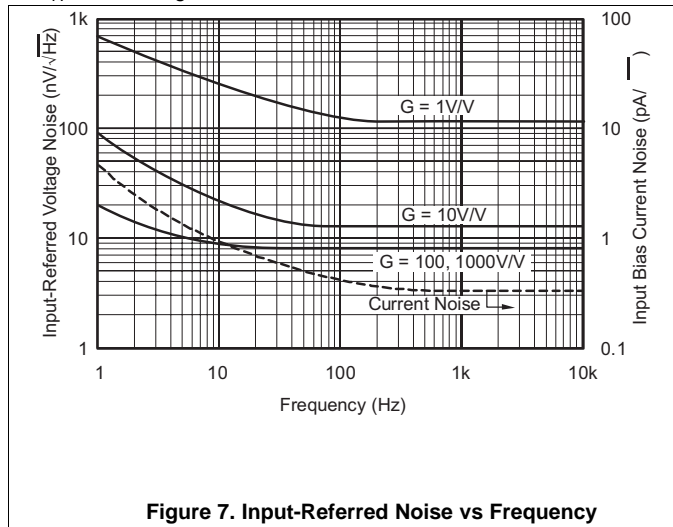


Figure 6. Input Common-Mode Range vs Output Voltage,  $V_S = \pm 5\text{ V}, \pm 2.5\text{ V}$

Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , unless otherwise noted.





Typical Characteristics (continued)

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , unless otherwise noted.

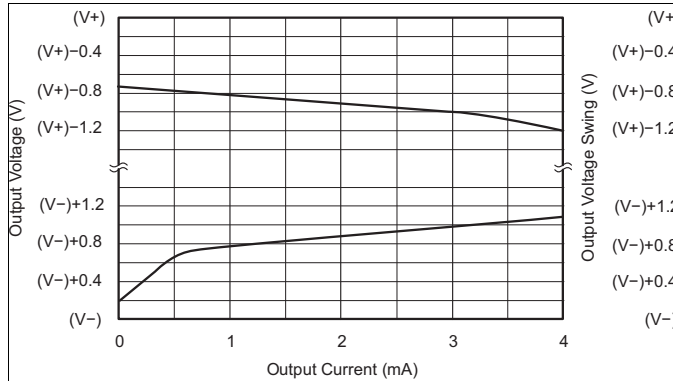


Figure 13. Output Voltage Swing vs Output Current

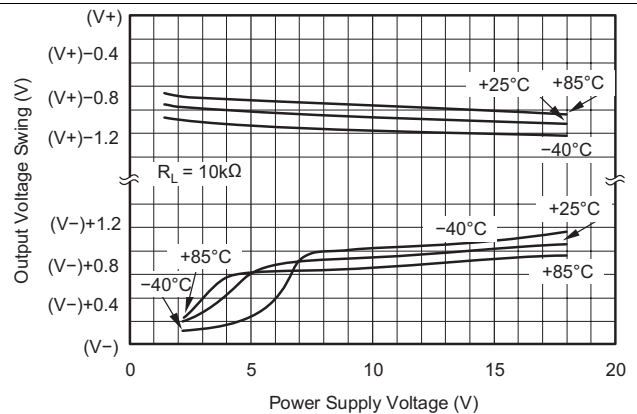


Figure 14. Output Voltage Swing vs Power Supply Voltage

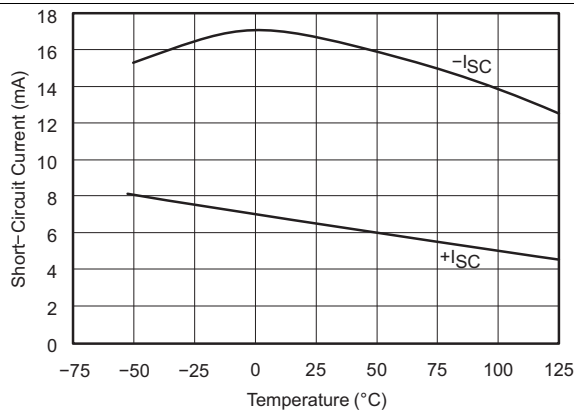


Figure 15. Short Circuit Output Current vs Temperature

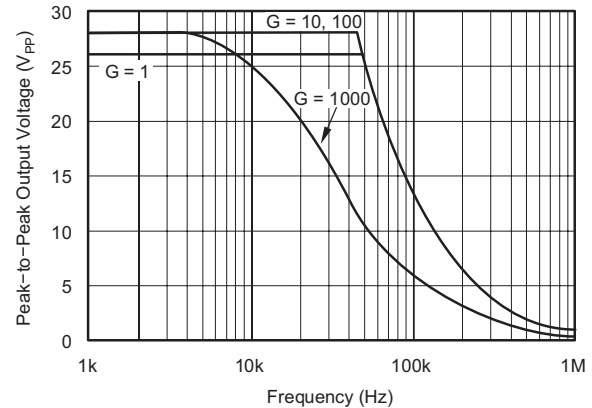


Figure 16. Maximum Output Voltage vs Frequency

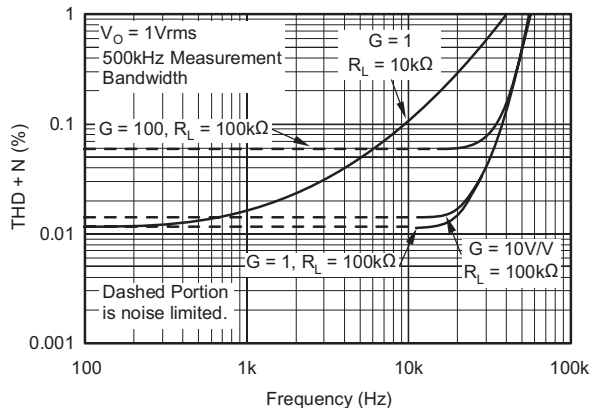


Figure 17. Total Harmonic Distortion + Noise vs Frequency

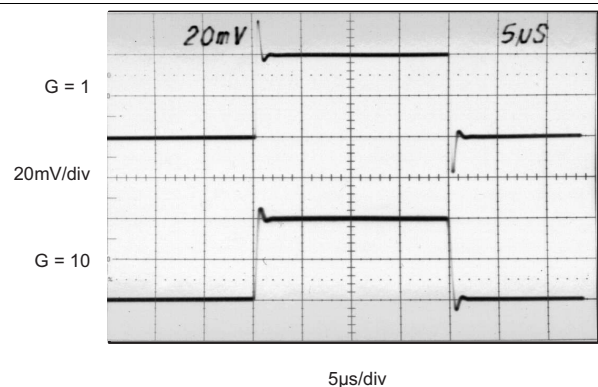
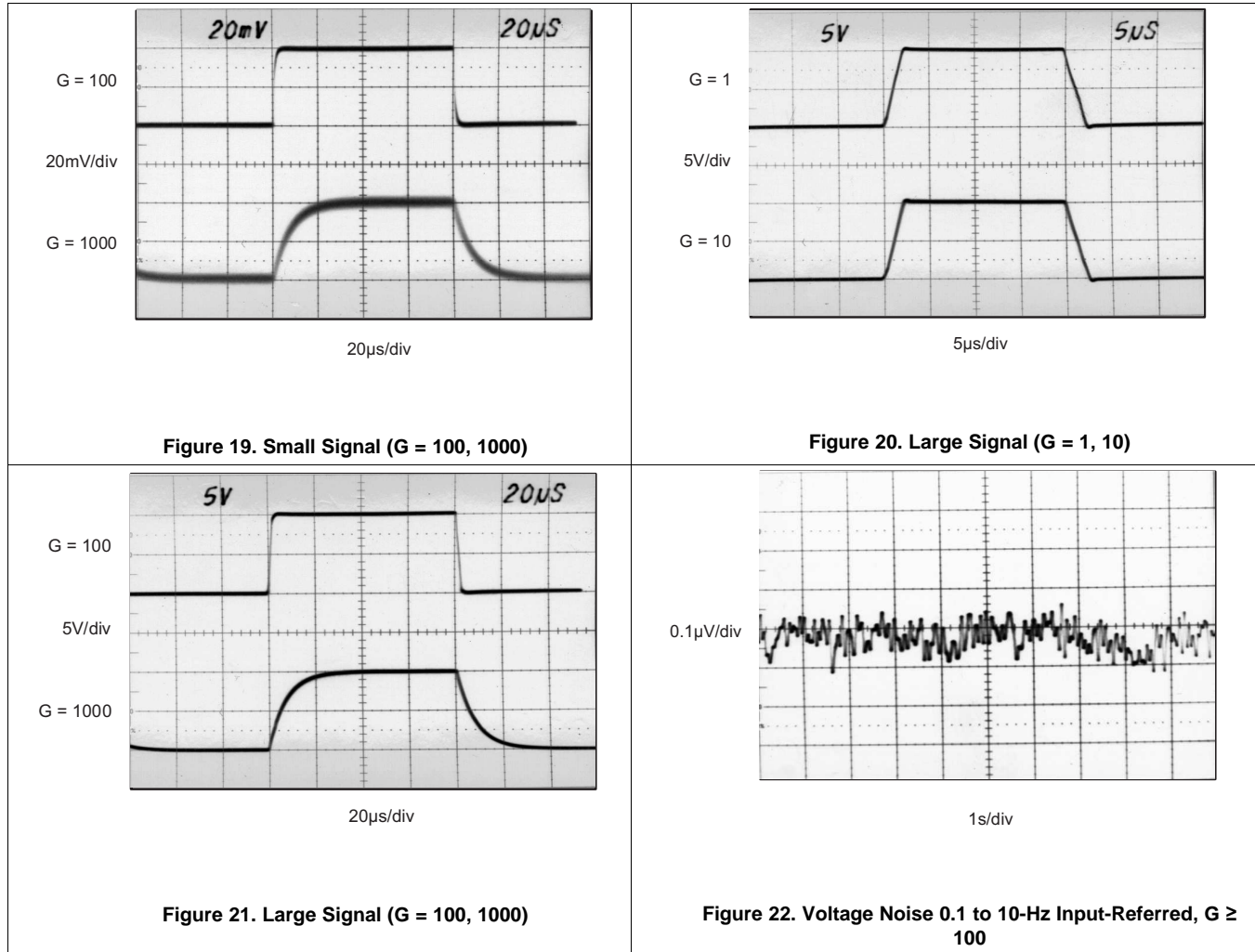


Figure 18. Small Signal (G = 1, 10)

**Typical Characteristics (continued)**

At  $T_A = 25^\circ\text{C}$ ,  $V_S = \pm 15\text{ V}$ , unless otherwise noted.

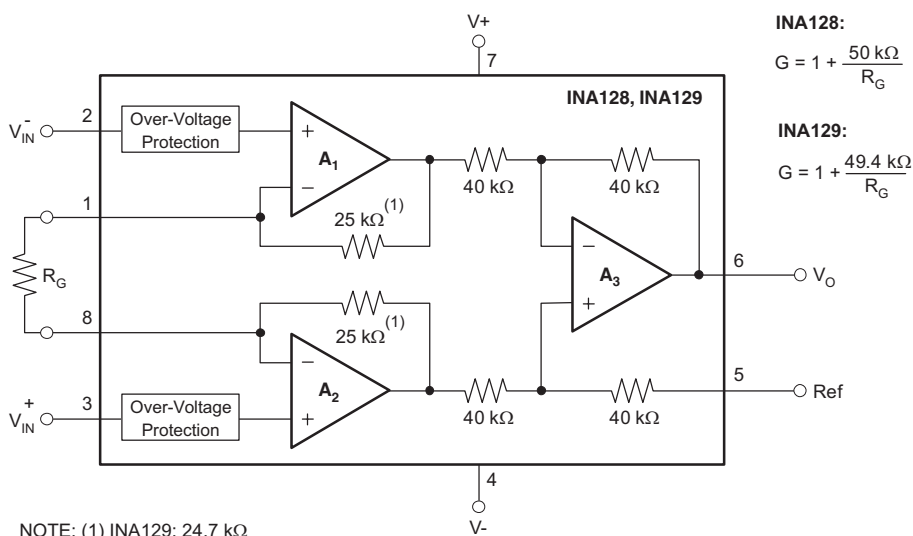


## 7 Detailed Description

### 7.1 Overview

The INA12x instrumentation amplifier is a type of differential amplifier that has been outfitted with input protection circuit and input buffer amplifiers, which eliminate the need for input impedance matching and make the amplifier particularly suitable for use in measurement and test equipment. Additional characteristics of the INA128 include a very low DC offset, low drift, low noise, very high open-loop gain, very high common-mode rejection ratio, and very high input impedances. The INA12x is used where great accuracy and stability of the circuit both short and long term are required.

### 7.2 Functional Block Diagram



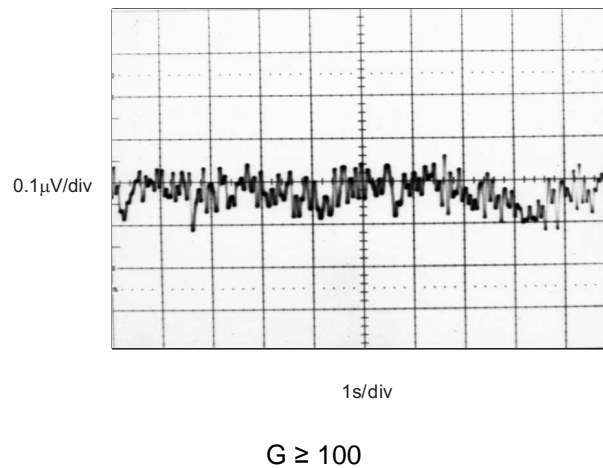
### 7.3 Feature Description

The INA12x devices are low power, general-purpose instrumentation amplifiers offering excellent accuracy. The versatile three-operational-amplifier design and small size make the amplifiers ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth, even at high gain. A single external resistor sets any gain from 1 to 10,000. The INA128 is laser trimmed for very low offset voltage (25  $\mu\text{V}$  typical) and high common-mode rejection (93 dB at  $G \geq 100$ ). These devices operate with power supplies as low as  $\pm 2.25 \text{ V}$ , and quiescent current of 2 mA, typically. The internal input protection can withstand up to  $\pm 40 \text{ V}$  without damage.

### 7.4 Device Functional Modes

#### 7.4.1 Noise Performance

The INA12x provides very low noise in most applications. Low-frequency noise is approximately  $0.2 \mu\text{V}_{\text{PP}}$  measured from 0.1 to 10 Hz ( $G \geq 100$ ). This provides dramatically improved noise when compared to state-of-the-art chopper-stabilized amplifiers.

**Device Functional Modes (continued)**

**Figure 23. 0.1-Hz to 10-Hz Input-Referred Voltage Noise**
**7.4.2 Input Common-Mode Range**

The linear input voltage range of the input circuitry of the INA12x is from approximately 1.4 V below the positive supply voltage to 1.7 V above the negative supply. As a differential input voltage causes the output voltage increase, however, the linear input range is limited by the output voltage swing of amplifiers  $A_1$  and  $A_2$ . Thus the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage (see performance curve [Figure 6](#)).

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of  $A_3$  will be near 0 V even though both inputs are overloaded.

## 8 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 8.1 Application Information

The INA12x measures small differential voltage with high common-mode voltage developed between the noninverting and inverting input. The high-input voltage protection circuit in conjunction with high input impedance make the INA12x suitable for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations.

### 8.2 Typical Application

Figure 24 shows the basic connections required for operation of the INA12x. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown. The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 8 Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR ( $G = 1$ ).

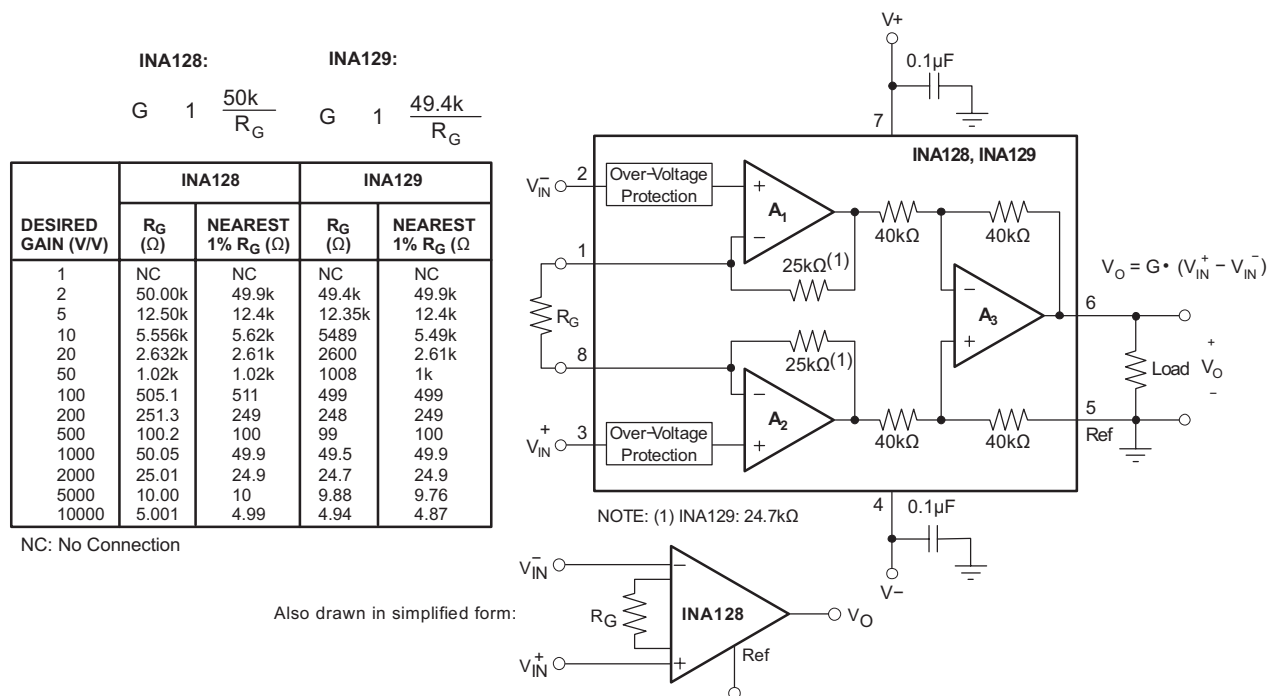


Figure 24. Basic Connections

#### 8.2.1 Design Requirements

The device can be configured to monitor the input differential voltage when the gain of the input signal is set by the external resistor  $R_G$ . The output signal references to the Ref pin. The most common application is where the output is referenced to ground when no input signal is present by connecting the Ref pin to ground, as Figure 24 shows. When the input signal increases, the output voltage at the OUT pin increases, too.

## Typical Application (continued)

### 8.2.2 Detailed Design Procedure

#### 8.2.2.1 Setting the Gain

Gain is set by connecting a single external resistor,  $R_G$ , connected between pins 1 and 8:

$$\text{INA128: } g = 1 + 50 \text{ k}\Omega / R_G \quad (1)$$

Commonly used gains and resistor values are shown in [Figure 24](#).

The 50-k $\Omega$  term in [Equation 1](#) comes from the sum of the two internal feedback resistors of  $A_1$  and  $A_2$ . These on-chip metal film resistors are laser-trimmed to accurate absolute values. The accuracy and temperature coefficient of these internal resistors are included in the gain accuracy and drift specifications of the INA128.

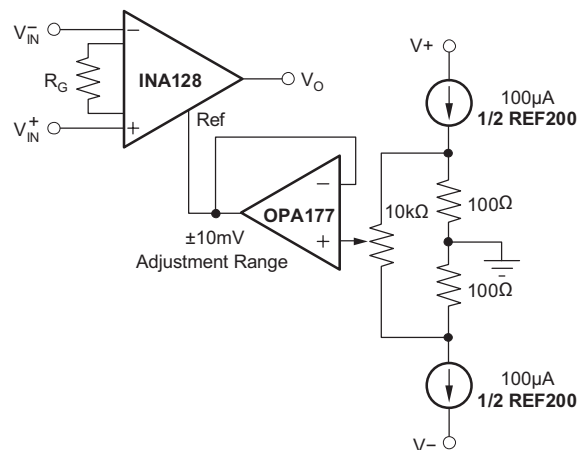
The stability and temperature drift of the external gain setting resistor,  $R_G$ , also affects gain.  $R_G$ 's contribution to gain accuracy and drift can be directly inferred from [Equation 1](#). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance, which contributes additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

#### 8.2.2.2 Dynamic Performance

The typical performance curve [Figure 1](#) shows that, despite its low quiescent current, the INA12x achieves wide bandwidth even at high gain. This is due to the current-feedback topology of the input stage circuitry. Settling time also remains excellent at high gain.

#### 8.2.2.3 Offset Trimming

The INA12x is laser-trimmed for low-offset voltage and offset voltage drift. Most applications require no external offset adjustment. [Figure 25](#) shows an optional circuit for trimming the output offset voltage. The voltage applied to the Ref terminal is summed with the output. The op amp buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.



**Figure 25. Optional Trimming of Output Offset Voltage**

#### 8.2.2.4 Input Bias Current Return Path

The input impedance of the INA12x is extremely high: approximately  $10^{10} \Omega$ . However, a path must be provided for the input bias current of both inputs. This input bias current is approximately  $\pm 2 \text{ nA}$ . High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. [Figure 26](#) shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range, and the input amplifiers will saturate.

### Typical Application (continued)

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 26). With higher source impedance, using two equal resistors provides a balanced input, with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

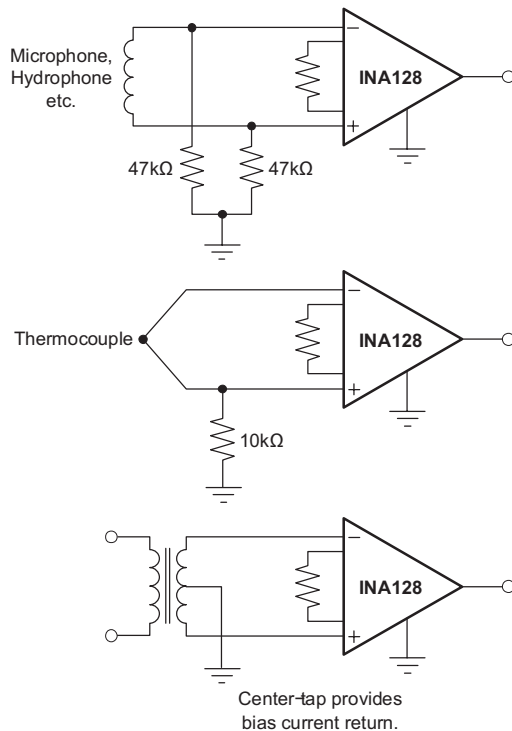
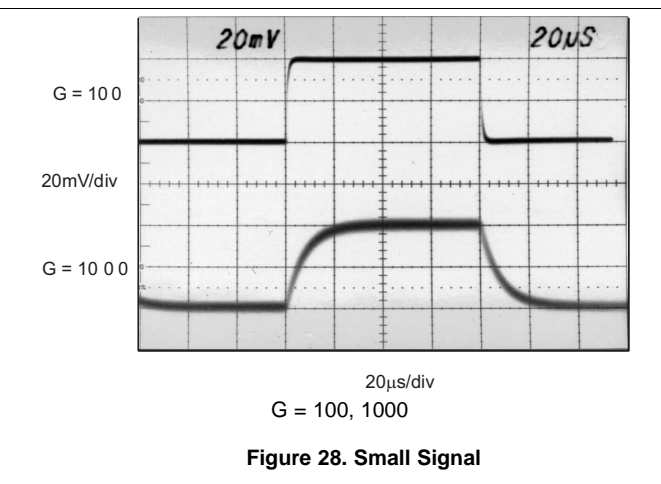
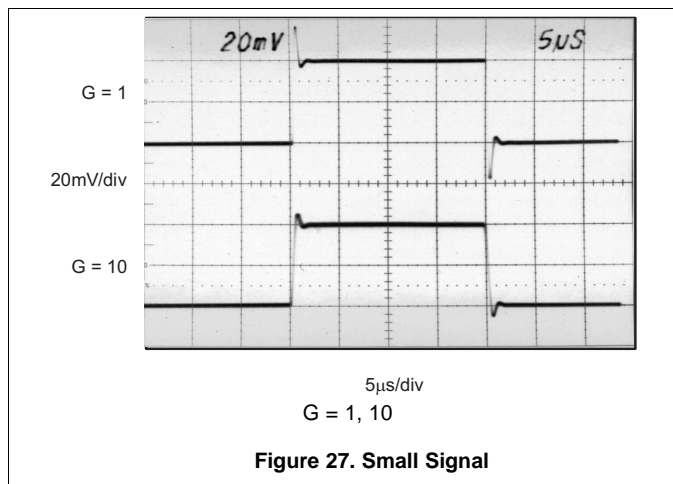
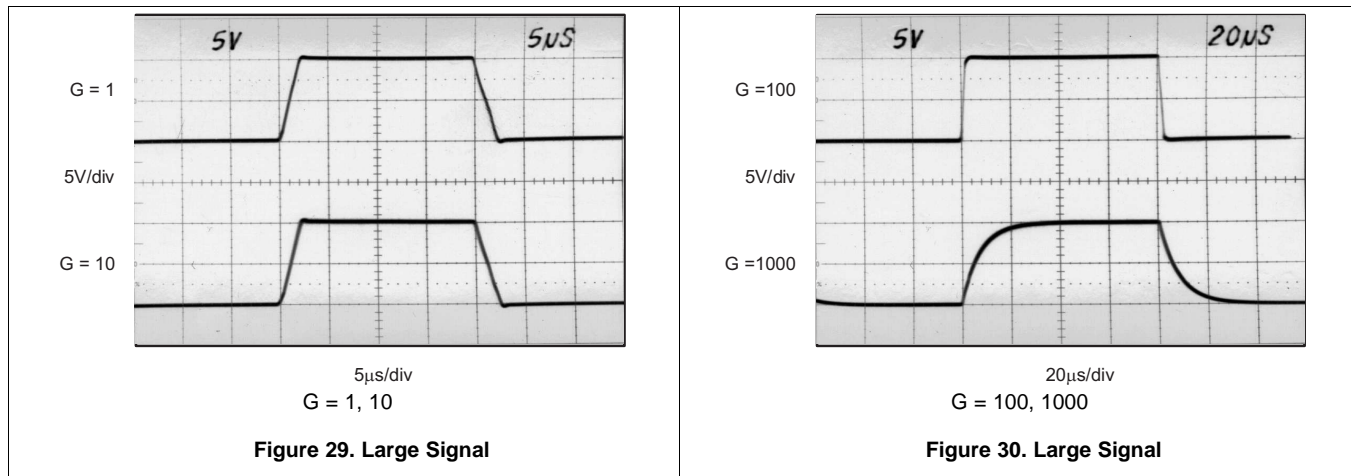


Figure 26. Providing an Input Common-Mode Current Path

### 8.2.3 Application Curves





**Typical Application (continued)**


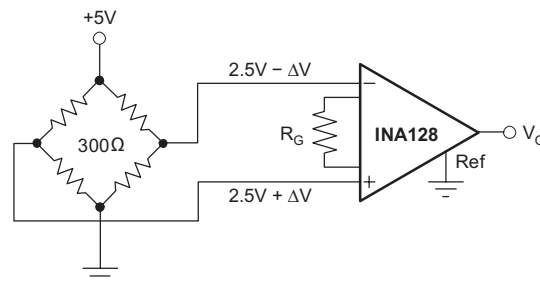
## 9 Power Supply Recommendations

The minimum power supply voltage for INA12x is  $\pm 2.25$  V and the maximum power supply voltage is  $\pm 18$  V. This minimum and maximum range covers a wide range of power supplies; but for optimum performance,  $\pm 15$  V is recommended. TI recommends adding a bypass capacitor at the input to compensate for the layout and power supply source impedance.

### 9.1 Low Voltage Operation

The INA12x can be operated on power supplies as low as  $\pm 2.25$  V. Performance remains excellent with power supplies ranging from  $\pm 2.25$  V to  $\pm 18$  V. Most parameters vary only slightly throughout this supply voltage range—see [Typical Characteristics](#).

Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. [Figure 6](#) shows the range of linear operation for  $\pm 15$ -V,  $\pm 5$ -V, and  $\pm 2.5$ -V supplies.



**Figure 31. Bridge Amplifier**



Low Voltage Operation (continued)

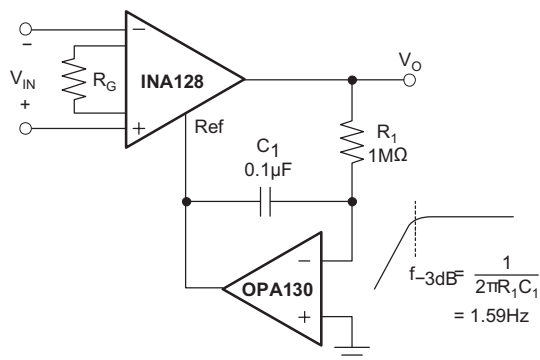
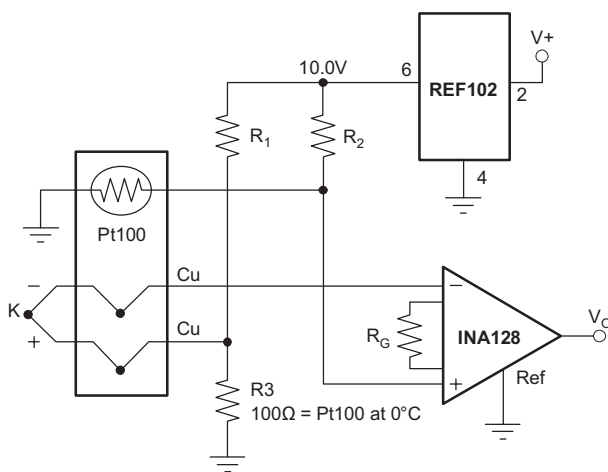


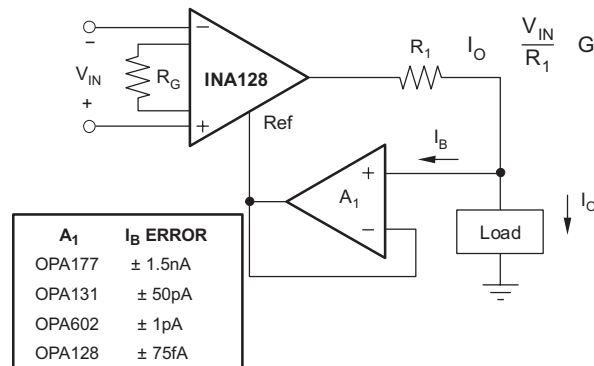
Figure 32. AC-Coupled Instrumentation Amplifier



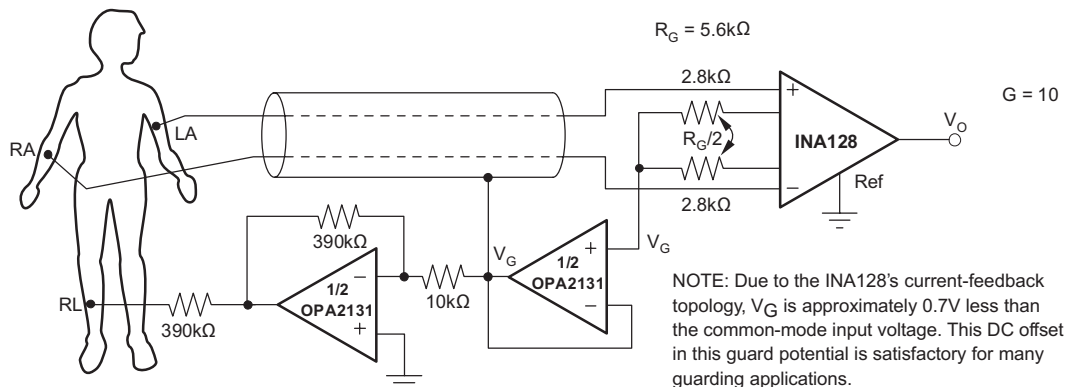
ISA TYPE	MATERIAL	SEEBECK COEFFICIENT ( μV/°C)	R <sub>1</sub> , R <sub>2</sub>
E	+ Chromel - Constantan	58.5	66.5kΩ
J	+ Iron - Constantan	50.2	76.8kΩ
K	+ Chromel - Alumel	39.4	97.6kΩ
T	+ Copper - Constantan	38.0	102kΩ

Figure 33. Thermocouple Amplifier with RTD Cold-Junction Compensation

## Low Voltage Operation (continued)



**Figure 34. Differential Voltage to Current Converter**



**Figure 35. ECG Amplifier with Right-Leg Drive**

## 10 Layout

### 10.1 Layout Guidelines

Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1  $\mu\text{F}$  to 1  $\mu\text{F}$ . If necessary, additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. These decoupling capacitors must be placed between the power supply and INA12x devices.

The gain resistor must be placed close to pin 1 and pin 8. This placement limits the layout loop and minimizes any noise coupling into the part.

## 10.2 Layout Example

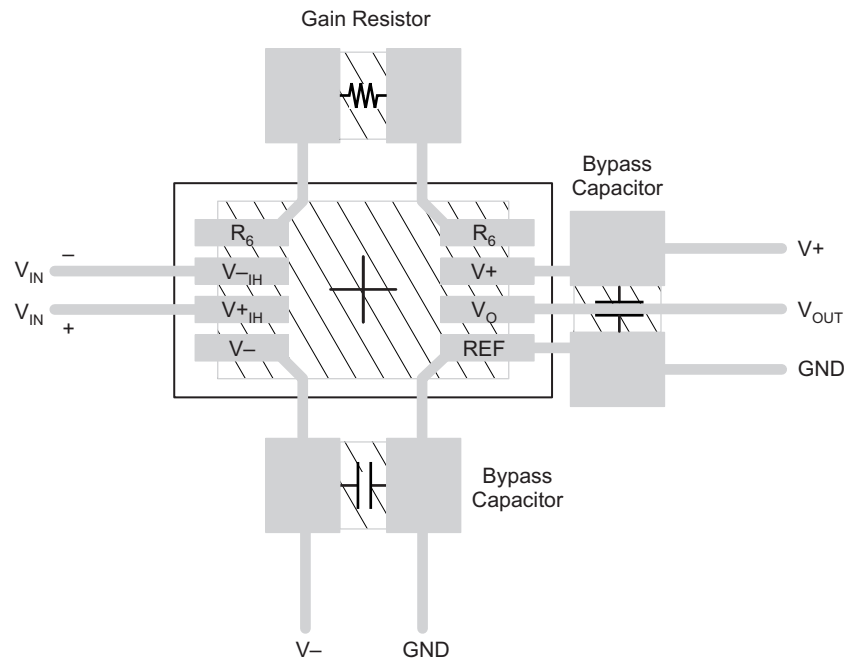


Figure 36. Recommended Layout

## 11 Device and Documentation Support

### 11.1 Community Resources

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**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At [e2e.ti.com](http://e2e.ti.com), you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 1. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
INA128	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
INA129	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 11.3 Trademarks

E2E is a trademark of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 11.5 Glossary

**SLYZ022** — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA128P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA128P	<a href="#">Samples</a>
INA128PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA128P A	<a href="#">Samples</a>
INA128PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA128P A	<a href="#">Samples</a>
INA128PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA128P	<a href="#">Samples</a>
INA128U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 128U	<a href="#">Samples</a>
INA128U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 128U	<a href="#">Samples</a>
INA128U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 128U	<a href="#">Samples</a>
INA128UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 128U A	<a href="#">Samples</a>
INA128UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 128U A	<a href="#">Samples</a>
INA128UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 128U A	<a href="#">Samples</a>
INA128UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 128U A	<a href="#">Samples</a>
INA128UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 128U A	<a href="#">Samples</a>
INA128UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 128U A	<a href="#">Samples</a>
INA128UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 128U	<a href="#">Samples</a>

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA129P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA129P	<a href="#">Samples</a>
INA129PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA129P A	<a href="#">Samples</a>
INA129PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA129P A	<a href="#">Samples</a>
INA129PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type		INA129P	<a href="#">Samples</a>
INA129U	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 129U	<a href="#">Samples</a>
INA129U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 129U	<a href="#">Samples</a>
INA129U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 129U	<a href="#">Samples</a>
INA129UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 129U A	<a href="#">Samples</a>
INA129UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 129U A	<a href="#">Samples</a>
INA129UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 129U A	<a href="#">Samples</a>
INA129UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 129U A	<a href="#">Samples</a>
INA129UAE4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 125	INA 129U A	<a href="#">Samples</a>
INA129UG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR		INA 129U	<a href="#">Samples</a>

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**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

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**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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#### **OTHER QUALIFIED VERSIONS OF INA128, INA129 :**

- Enhanced Product: [INA129-EP](#)

NOTE: Qualified Version Definitions:

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

## TAPE AND REEL INFORMATION



### QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
INA128U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA128UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA129U/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
INA129UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1



**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
INA128U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA128UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA129U/2K5	SOIC	D	8	2500	367.0	367.0	35.0
INA129UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0

P (R-PDIP-T8)

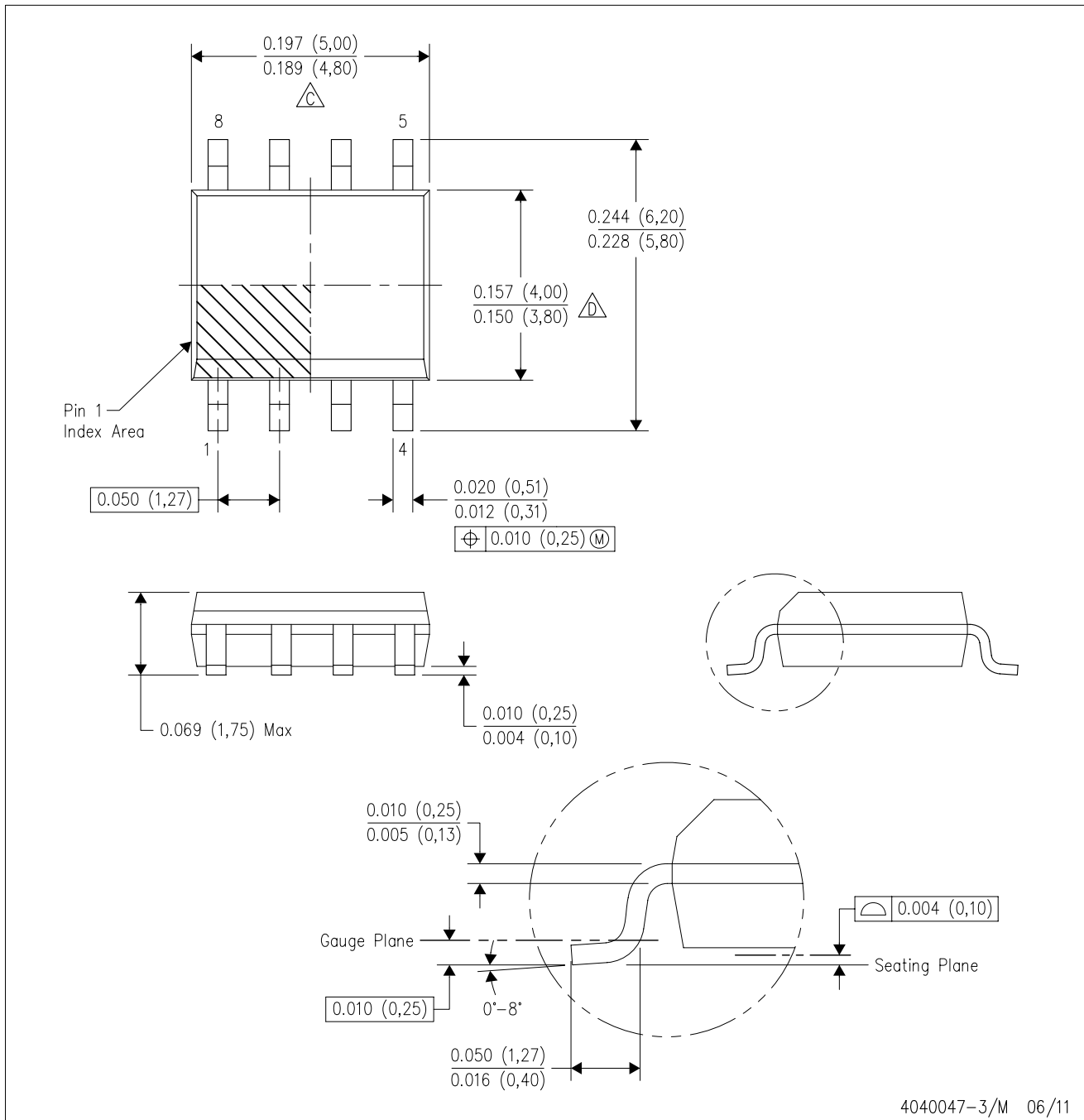
PLASTIC DUAL-IN-LINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001 variation BA.

D (R-PDSO-G8)

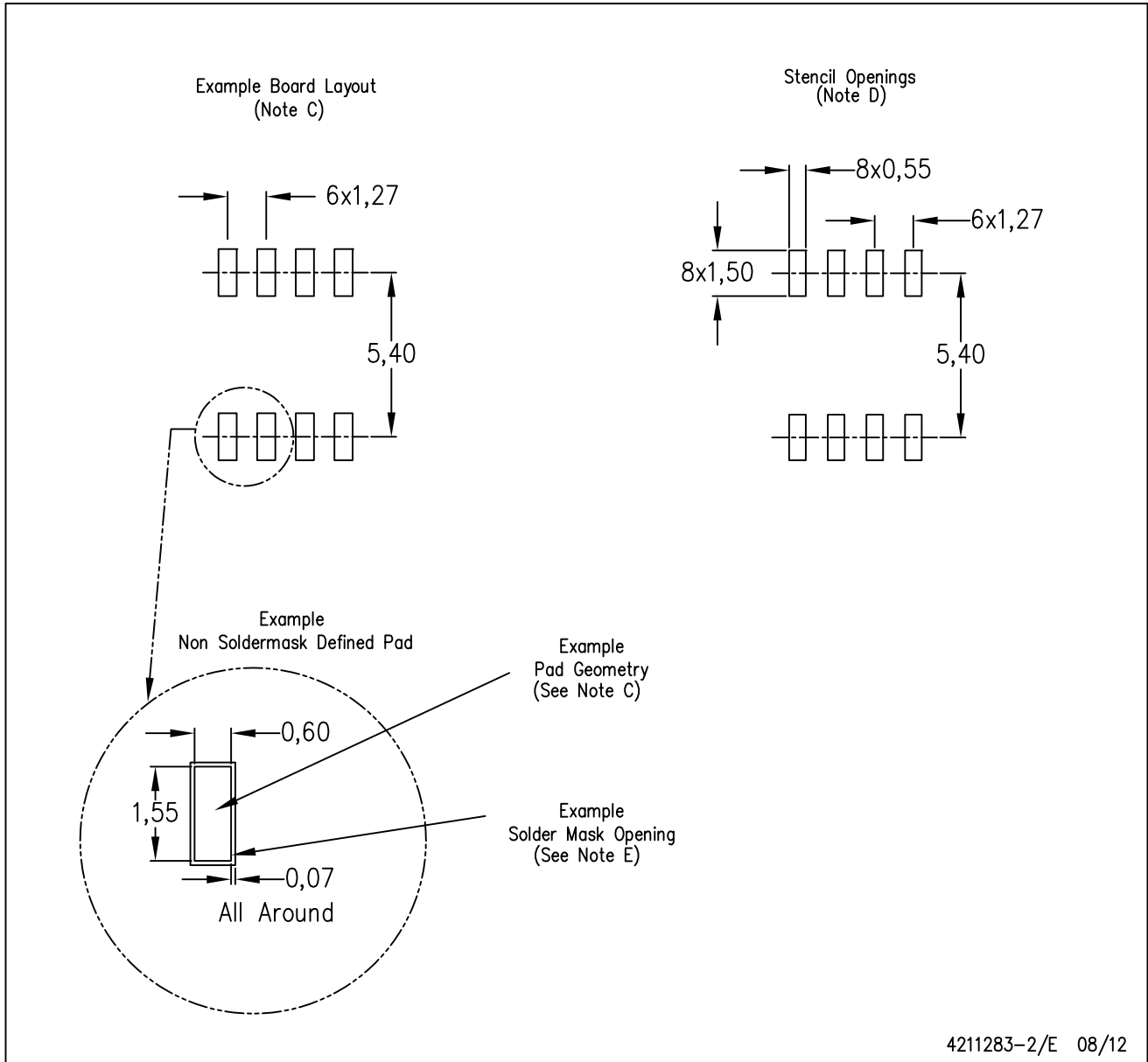
PLASTIC SMALL OUTLINE



4040047-3/M 06/11

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
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  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>
Clocks and Timers	<a href="http://www.ti.com/clocks">www.ti.com/clocks</a>
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Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>
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OMAP Applications Processors	<a href="http://www.ti.com/omap">www.ti.com/omap</a>
Wireless Connectivity	<a href="http://www.ti.com/wirelessconnectivity">www.ti.com/wirelessconnectivity</a>

### Applications

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Computers and Peripherals	<a href="http://www.ti.com/computers">www.ti.com/computers</a>
Consumer Electronics	<a href="http://www.ti.com/consumer-apps">www.ti.com/consumer-apps</a>
Energy and Lighting	<a href="http://www.ti.com/energy">www.ti.com/energy</a>
Industrial	<a href="http://www.ti.com/industrial">www.ti.com/industrial</a>
Medical	<a href="http://www.ti.com/medical">www.ti.com/medical</a>
Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
Space, Avionics and Defense	<a href="http://www.ti.com/space-avionics-defense">www.ti.com/space-avionics-defense</a>
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